

An Overview of SVX4 Testing

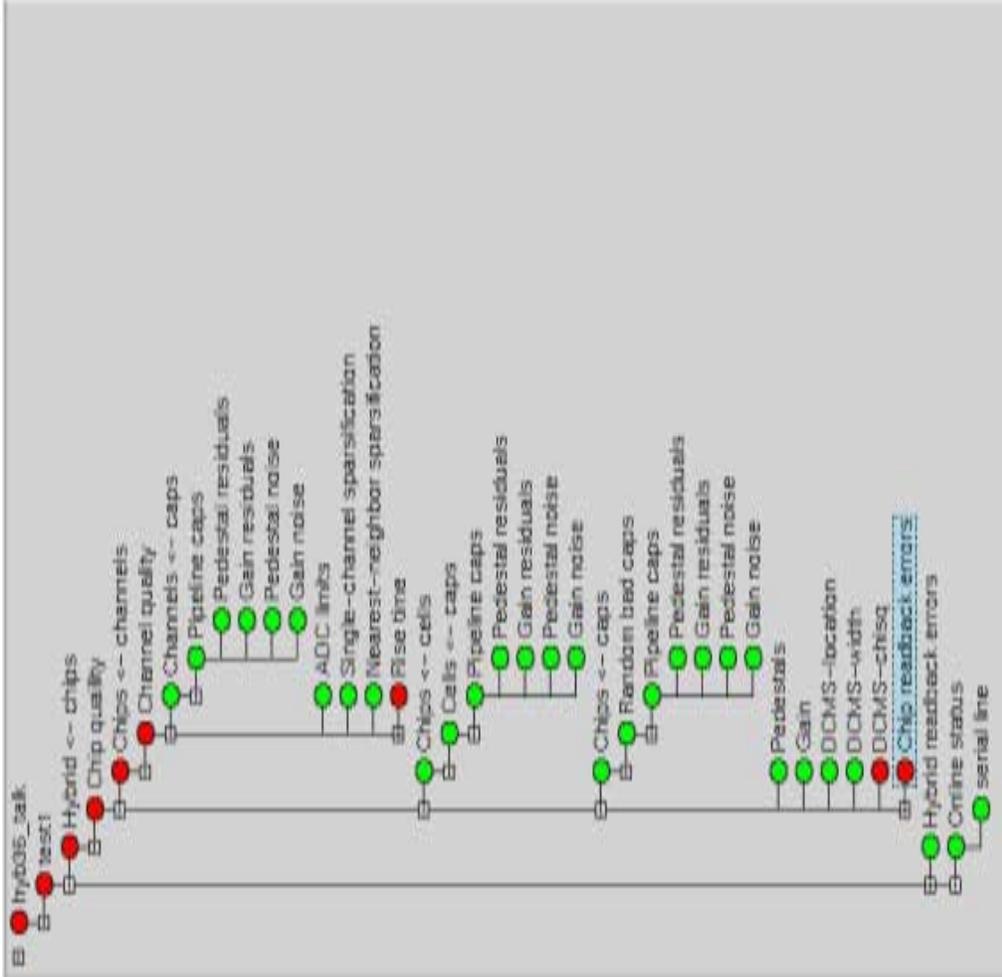
John Freeman, 4/2/03

The Htwish Test Program

- We're currently working with the Htwish program, originally written by Igor Volobouev to test SVX3 hybrids
- Htwish has been modified to provide rapid, comprehensive tests of SVX4 hybrids
- But our job is not yet complete...

Where We're Going

- We want to expand Htwish's test suite to make the program even more comprehensive
- In this talk, I'll discuss current Htwish tests, as well as some we may add (primarily taken from wafer testing)



Update: Hybrid readback errors

Type : Value : Save Dismiss

Test pass status :

- Pass
- Some problems
- Fail
- Undefined
- No test data

First Things First: Currents

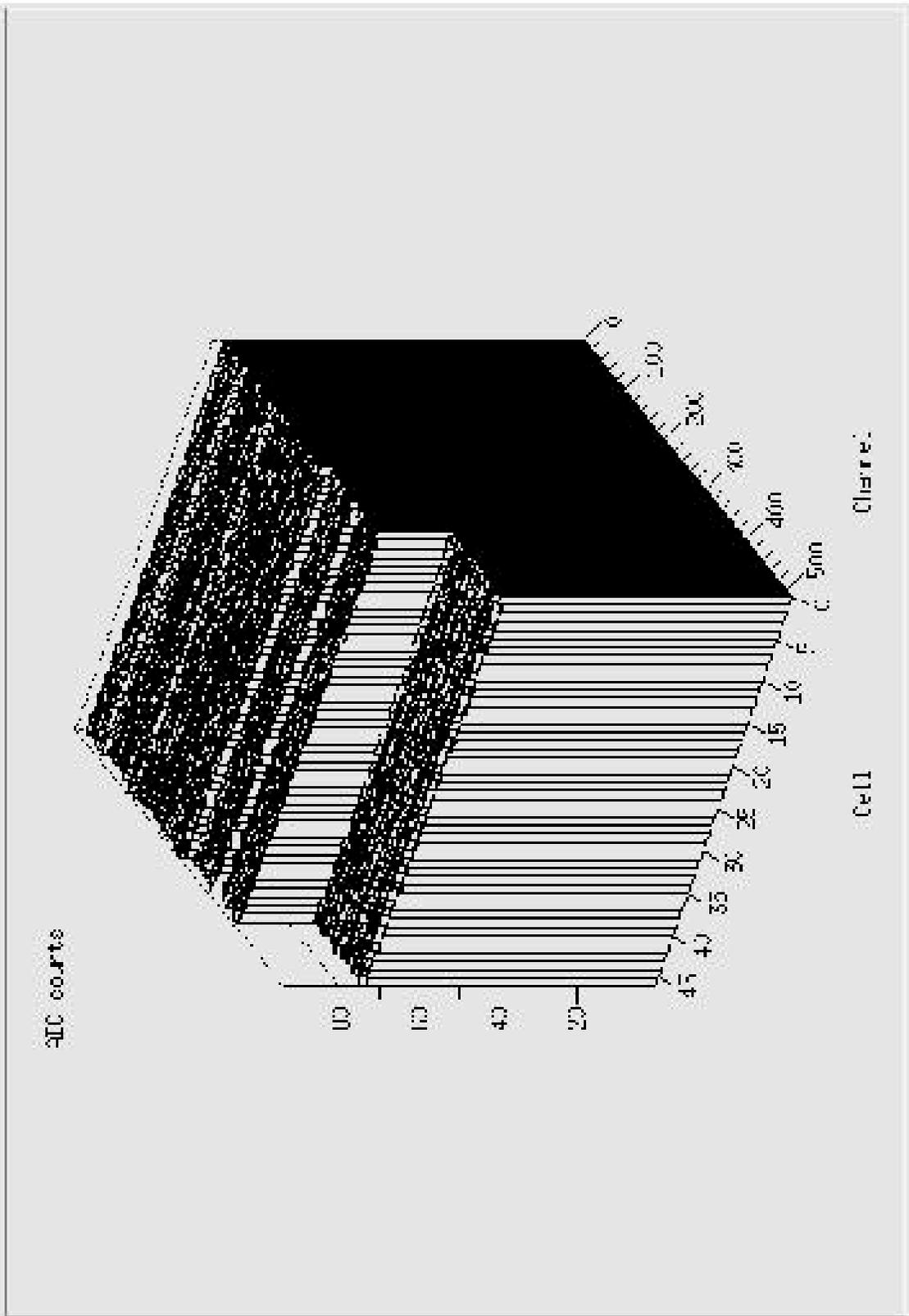
- Testing currents involves several measurements of both the digital and analog currents during the testing procedure
- If any shorts are discovered, the chip (and hybrid's) failure is automatic

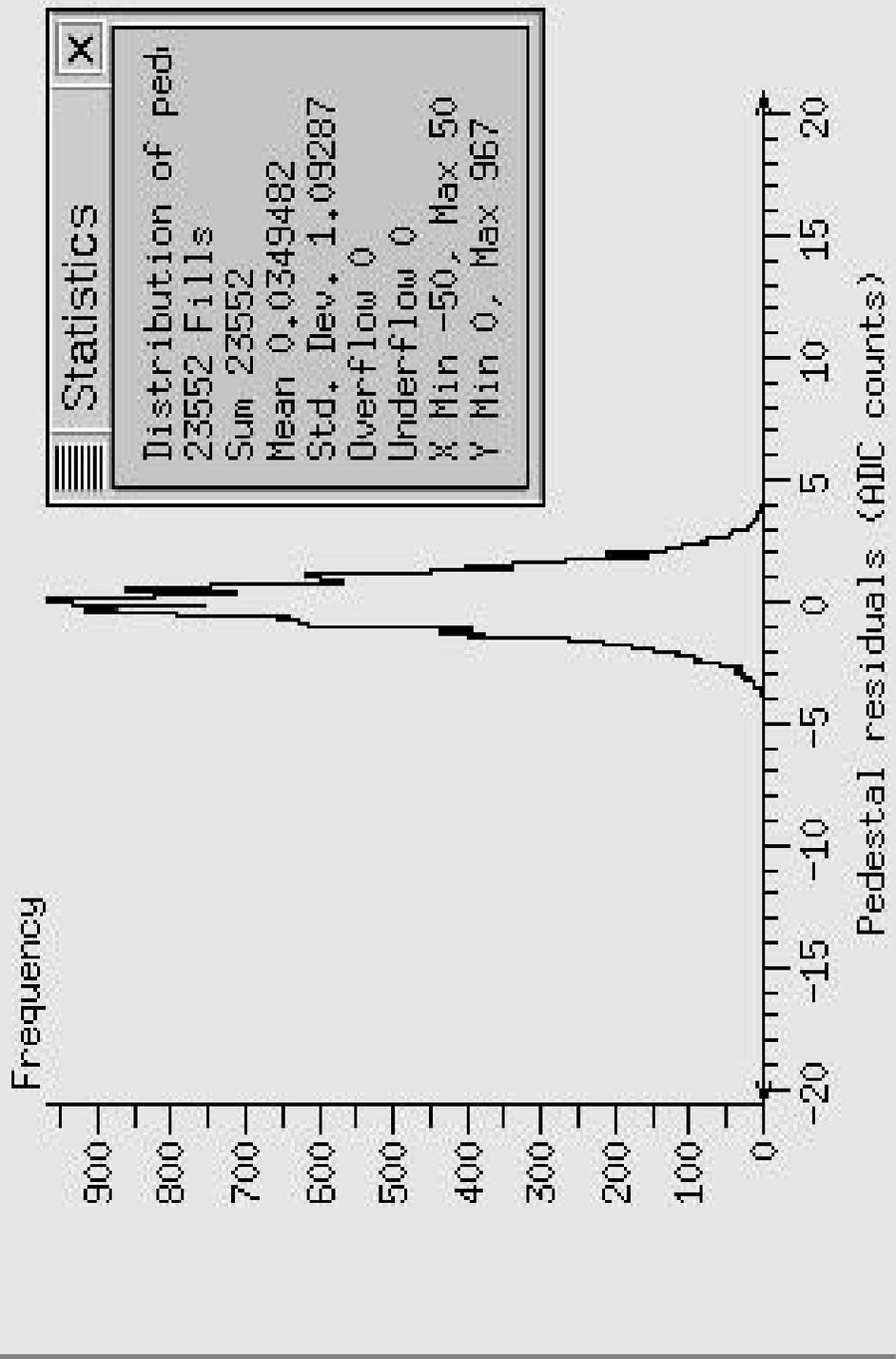
Line Tests

- Serial line test: Initialize the hybrid with 0's, then 1's, then 0's again. Make sure we read out what we expect on the priority-out line— there should be no bits stuck in the shift register
- Neighbor logic: Make sure top and bottom neighbor behave as expected during digitize

Pipeline Pedestal Tests

- Very fundamental– simply examine ADC value of non-injected channels
- Htwish looks at all $128*46$ pipeline capacitors on a chip => very thorough testing!
- Examine pedestal uniformity across a chip, noise, look for bow structures, etc.





Pedestal Tests, Cont'd

- Adjust ramp pedestal initialization bits over all 16 possible values
- For each ramp value, find the chip's median pedestal value, and the residuals of the other channels
- This allows us to examine the effect of the initial ramp setting on pedestal uniformity

Multiple Events

- Use four closely spaced L1A triggers to see if chip can properly store four events in its pipeline
- Also of interest is how the pedestal structure varies over these four events

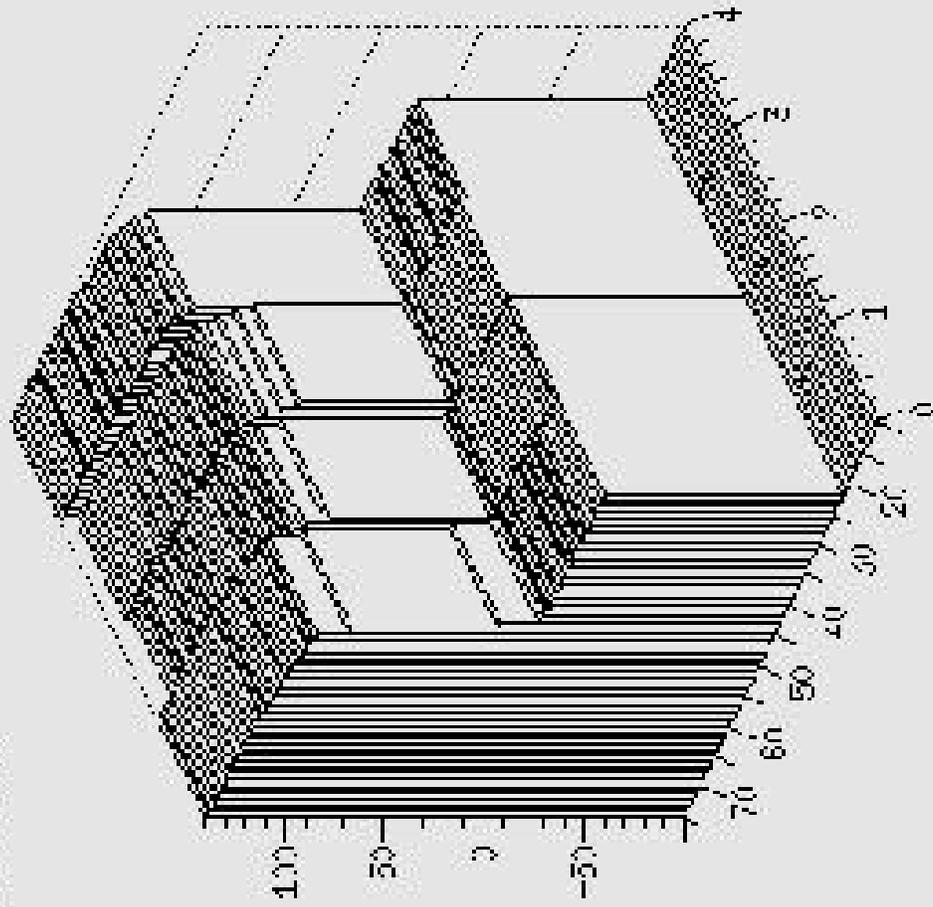
Gain Tests

- Read out each channel at different values of charge injection, and calculate the ADC count / voltage slope (= “gain”)
- Gain similar to pedestal in that every pipeline cap has its own gain value => some analysis similar to pedestal analysis
- Additionally: study of gain linearity / fluctuations in specific pipeline capacitors

Dynamic Common Mode Suppression

- Idea is to see how many channels on a chip need to be injected before chip is fooled into subtracting off the injected, rather than the pedestal, channels
- We have doubts as to the “fairness” of this test

HDC courts



Channel at Fccrystal Chip number

Sparsification Tests

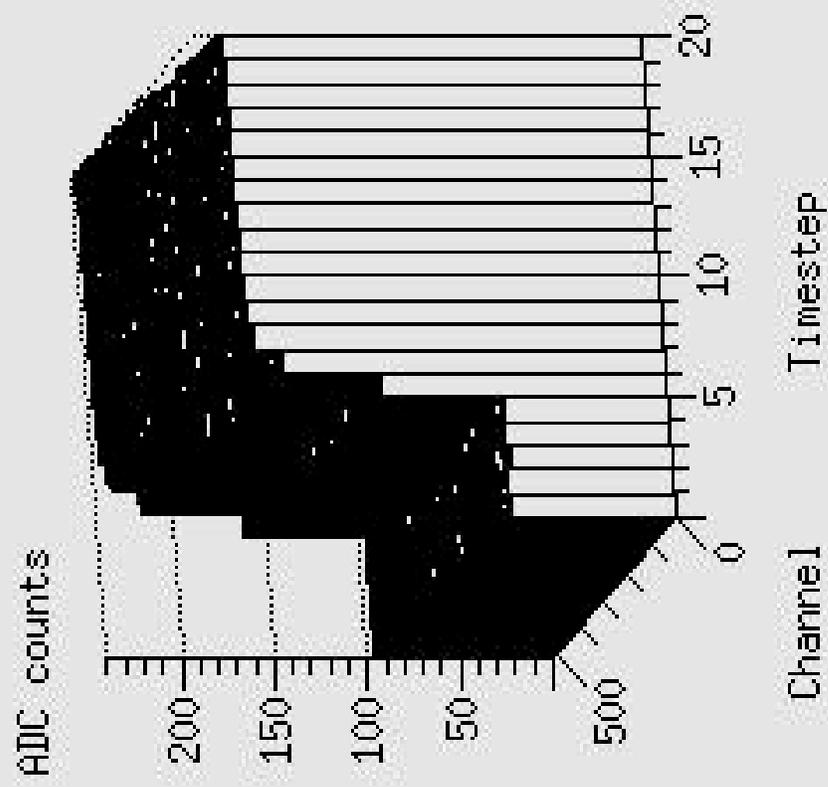
- Most fundamental: inject charge into specific channels, and make sure you read out the channels you expect (with and w/out read-neighbor set)

Other Sparsification Tests

- Sparsification S-Curve : Increase readout threshold from well below to well above pedestal value; then fit S-Curve to the # of channels read out vs. the readout threshold
- Sparsification effect on readout value– look at the value of injected channels both with and without read-all flag set

Preamp Risetime

- This test examines the preamp speed given different preamp bandwidths
- We don't access the analog output of the preamp, but vary the time of charge injection within an FE bucket



Pipeline Delay

- With the L1A trigger in a fixed bucket, step the trigger latency over a large range of values (42), and check cell ID each time
- This is done for every cell in the pipeline – exhaustive check of the pipeline pointer!

ADC Latch

- Test to insure that no bits are stuck in our ADC latches
- Use different settings of counter modulo (some of which will be complementary in Gray code)
- Make sure counter modulo value always gets read out in every channel

Deadtimeless Operation

- Examine the SVX4's deadtimeless abilities by initiating a readout sequence with a “dummy” trigger, and then triggering on a specific bucket during readout
- Buckets looked at by Htwish cover all of digitize, as well as beginning and end of readout

Deadtimeless Operation (cont'd)

- Test is performed in three modes: “regular”, “charge-injected”, and “sparsified”
- In summary, we re-test many aspects of the chip, but with the deadtimeless twist added

Discussion

- We currently use many tests on our hybrids. But we can do more, and the question becomes:

Which tests can you think of that we should add?