I. SVX4_V1 Pin List (* = wire bonding not required for D0 mode chips)

| Pin Number | Pin Name | Type Analog Digital | Type Input Output | Nom. Voltage | Wire Bonded | Description & External Components Required |
|---|---|---|---|---|---|---|
| 1, 81 | VCAL | A | I | AVDDfe ÷ 4 | Either | Calibration charge voltage; Qinj = VCAL * 25 fF |
| 2, 80 | AVDDfe | A | I | 2.5 | Either | Frontend analog power supply— decouple to gnd! w/0.1 uF |
| 3, 79 | Bias | A | I | 0.8 | Either | Frontend master bias reference—decouple to AVDDfe w/10 nF |
| 4, 78 | VRset | A | I | 1.0 | No | Frontend reset level reference voltage |
| 5 | PreampBuf127 | A | O | -- | No | Ch127 preamp buffered output; requires ext resistor |
| 6 | Ncas | A | O | 0.6 | No | Preamp N-cascode bias voltage |
| 7, 8, 9, 14, 212 | gnd! | A | I | 0 | No | Analog ground, substrate |
| 10 | ReadBuf127 | A | O | -- | No | Ch127 Pipeline Read amplifier output; requires ext. resistor |
| 11 | WriteBuf127 | A | O | -- | No | Ch127 Pipeline Write amplifier output; requires external resistor |
| 12, 75 | QGND | A | I | 0 | Either | Pipeline sample switch gnd |
| 13, 74 | QVDD | A | I | 2.5 | Either | Pipeline sample switch vdd |
| 15, 73 | AREF | A | I | 2.5 | Either | ADC ramp pedestal DAC reference |
| 16, 72 | AVDDadc | A | I | 2.5 | Either | ADC analog supply |
| 17, 71 | IQUI | A | I | 0.6 | Either | ADC and data receiver bias current setting—7.7k resistor to AVDDadc |
| 18, 70 | VTH | A | I | 0.9 | Either | Dynamic Pedestal Subtraction threshold voltage setting |
| 19, 69, 77 | gndd! | A | I | 0 | Either 19 or 69 | Digital ground |
| 20, 68, 76 | vddd! | A | I | 2.5 | Either 20 or 68 | Digital Vdd |
| 21, 67 | D0MODE | D | I | 0/2.5 | Either | Connect to vddd! for D0, gndd! for CDF |

| Pin Number | Pin Name | Analog Digital Diff | Input Output I/O | Nom. Voltage | Wire Bonded | Description & External Components Required |
|---|---|---|---|---|---|---|
| 22, 66 | USESEU | D | I | 0/2.5 | Either | Connect to vddd! to select SEU register for configuration, or gndd! for shift register output |
| 23, 65 | ISLOPE | A | I | 1.5 | Either | ADC ramp slope bias—36k resistor to gnd! |
| 24 | BNBR | D | I/O | 0/2.5 | Yes | Bottom Neighbor; open drain w/2k internal pull-up |
| 25 | PRIOUT | Diff | O | 0-2.5 | Yes | Priority Out plus |
| 26 | PRIOUTB | Diff | O | 0-2.5 | Yes | Priority Out minus |
| 27, 61 | SVDD | A | I | 2.5 | Either | Output Driver supply |
| 28, 60 | SGND | A | I | 0 | Either | Output Driver ground |
| 29 | EXTRA | -- | -- | -- | No | Spare pad |
| 30, 32, 34, 36, 38, 40, 42, 44 | BUSB<7>, .., BUSB<0> | Diff | I/O | 0-2.5 | Yes | Data bus 7—0 minus (see "Bus Pin Multiplexing Table" for secondary pin function by mode) |
| 31, 33, 35, 37, 39, 41, 43, 45 | BUS<7>, .., BUS<0> | Diff | I/O | 0-2.5 | Yes | Data bus 7—0 plus (see "Bus Pin Multiplexing Table" for secondary pin function by mode) |
| 46 | OBDVB | Diff | I/O | 0-2.5 | Yes | Odd Byte Data Valid minus |
| 47 | OBDV | Diff | I/O | 0-2.5 | Yes | Odd Byte Data Valid plus |
| 48, 210 | BECLKB | Diff | I | 0-2.5 | Either | Backend Clock minus |
| 49, 211 | BECLK | Diff | I | 0-2.5 | Either | Backend Clock plus |
| 50 | FECLKB | Diff | I | 0-2.5 | Either | Frontend Clock minus |
| 51 | FECLK | Diff | I | 0-2.5 | Either | Frontend Clock plus |
| 52 | CHMODE | D | I | 0/2.5 | Yes | Change Mode |
| 53 | BEMODE | D | I | 0/2.5 | Yes | Backend Mode (Mode 1) |
| 54 | FEMODE | D | I | 0/2.5 | Yes | Frontend Mode (Mode 0) |
| 55 | CALSR | D | I | 0/2.5 | Yes* | Cal Strobe (Acquire mode) Write SEU reg (Initialize) |
| 56 | L1A | D | I | 0/2.5 | Yes* | Level 1 Accept |
| 57 | PIPERD2 | D | I | 0/2.5 | Yes* | Pipeline Read 2 |
| 58 | PIPERD1 | D | I | 0/2.5 | Yes* | Pipeline Read 1 |
| 59 | PARST | D | I | 0/2.5 | Yes* | Preamp Reset |
| 62 | PRIINB | Diff | O | 0-2.5 | Yes | Priority In minus |
| 63 | PRIIN | Diff | O | 0-2.5 | Yes | Priority In plus |
| 64 | TNBR | D | I/O | 0/2.5 | Yes | Top Neighbor; open drain w/2k internal pull-up |
| 82-209 | In<0—127> | A | I | 0.45 | Yes | Detector Inputs |

## II. SVX4_V2 Pin List (* = wire bonding not required for D0 mode chips)

| Pin Number | Pin Name | Type Analog Digital | Type Input Output | Nom. Voltage | Wire Bonded | Description & External Components Required |
|---|---|---|---|---|---|---|
| 1, 79 | VCAL | A | I | AVDDfe ÷ 4 | Either | Calibration charge setting |
| 2, 15, 71, 78 | AVDD | A | I | 2.5 | Either | Analog power supply—decouple to gnd! w/0.1 uF |
| 3, 77 | Bias | A | I | 0.8 | Either | Frontend master bias reference—decouple to AVDDfe w/10 nF |
| 4, 76 | VRset | A | I | 1.0 | No | Frontend reset level reference voltage |
| 5 | PreampBuf127 | A | O | -- | No | Ch127 preamp buffered output; requires ext resistor |
| 6 | Ncas | A | O | 0.6 | No | Preamp N-cascode bias voltage |
| 7, 8, 9, 12, 13, 75, 210 | gnd! | A | I | 0 | No | Analog ground, substrate |
| 10 | ReadBuf127 | A | O | -- | No | Ch127 Pipeline Read amplifier output; requires ext. resistor |
| 11 | WriteBuf127 | A | O | -- | No | Ch127 Pipeline Write amplifier output; requires external resistor |
| 14, 72 | AREF | A | I | 2.5 | Either | ADC ramp pedestal DAC reference |
| 16, 70 | IQUI | A | I | 0.6 | Either | ADC and data receiver bias current setting—7.7k resistor to AVDDadc |
| 17, 69 | VTH | A | I | 0.9 | Either | Dynamic Pedestal Subtraction threshold voltage setting |
| 18, 68, 74 | gndd! | A | I | 0 | Either 19 or 69 | Digital ground |
| 19, 67, 73 | vddd! | A | I | 2.5 | Either 20 or 68 | Digital Vdd |
| 20, 66 | D0MODE | D | I | 0/2.5 | Either | Connect to vddd! for D0, gndd! For CDF mode |
| 21, 65 | USESEU | D | I | 0/2.5 | Either | Connect to vddd! to select SEU register for configuration, or gndd! for shift register output |

| Pin Number | Pin Name | Analog Digital Diff | Input Output I/O | Nom. Voltage | Wire Bonded | Description & External Components Required |
|---|---|---|---|---|---|---|
| 22, 64 | ISLOPE | A | I | 1.5 | Either | ADC ramp slope bias—36k resistor to gnd! |
| 23 | BNBR | D | I/O | 0/2.5 | Yes | Bottom Neighbor; open drain w/2k internal pull-up |
| 24 | PRIOUT | Diff | O | 0-2.5 | Yes | Priority Out plus |
| 25 | PRIOUTB | Diff | O | 0-2.5 | Yes | Priority Out minus |
| 26, 60 | SVDD | A | I | 2.5 | Either | Output Driver supply |
| 27, 59 | SGND | A | I | 0 | Either | Output Driver ground |
| 28 | EXTRA | -- | -- | -- | No | Spare pad |
| 29, 31, 33, 35, 37, 39, 41, 43 | BUSB<7>, .., BUSB<0> | Diff | I/O | 0-2.5 | Yes | Data bus 7—0 minus (see "Bus Pin Multiplexing Table" for secondary pin function by mode) |
| 30, 32, 34, 36, 38, 40, 42, 44 | BUS<7>, .., BUS<0> | Diff | I/O | 0-2.5 | Yes | Data bus 7—0 plus (see "Bus Pin Multiplexing Table" for secondary pin function by mode) |
| 45 | OBDVB | Diff | I/O | 0-2.5 | Yes | Odd Byte Data Valid minus |
| 46 | OBDV | Diff | I/O | 0-2.5 | Yes | Odd Byte Data Valid plus |
| 47, 208 | BECLKB | Diff | I | 0-2.5 | Either | Backend Clock minus |
| 48, 209 | BECLK | Diff | I | 0-2.5 | Either | Backend Clock plus |
| 49 | FECLKB | Diff | I | 0-2.5 | Either | Frontend Clock minus |
| 50 | FECLK | Diff | I | 0-2.5 | Either | Frontend Clock plus |
| 51 | CHMODE | D | I | 0/2.5 | Yes | Change Mode |
| 52 | BEMODE | D | I | 0/2.5 | Yes | Backend Mode (Mode 1) |
| 53 | FEMODE | D | I | 0/2.5 | Yes | Frontend Mode (Mode 0) |
| 54 | CALSR | D | I | 0/2.5 | Yes* | Cal Strobe (Acquire mode) Write SEU reg (Initialize) |
| 55 | L1A | D | I | 0/2.5 | Yes* | Level 1 Accept |
| 56 | PIPERD2 | D | I | 0/2.5 | Yes* | Pipeline Read 2 |
| 57 | PIPERD1 | D | I | 0/2.5 | Yes* | Pipeline Read 1 |
| 58 | PARST | D | I | 0/2.5 | Yes* | Preamp Reset |
| 61 | PRIINB | Diff | O | 0-2.5 | Yes | Priority In minus |
| 62 | PRIIN | Diff | O | 0-2.5 | Yes | Priority In plus |
| 63 | TNBR | D | I/O | 0/2.5 | Yes | Top Neighbor; open drain w/2k internal pull-up |
| 80-207 | In<0—127> | A | I | 0.45 | Yes | Detector Inputs |