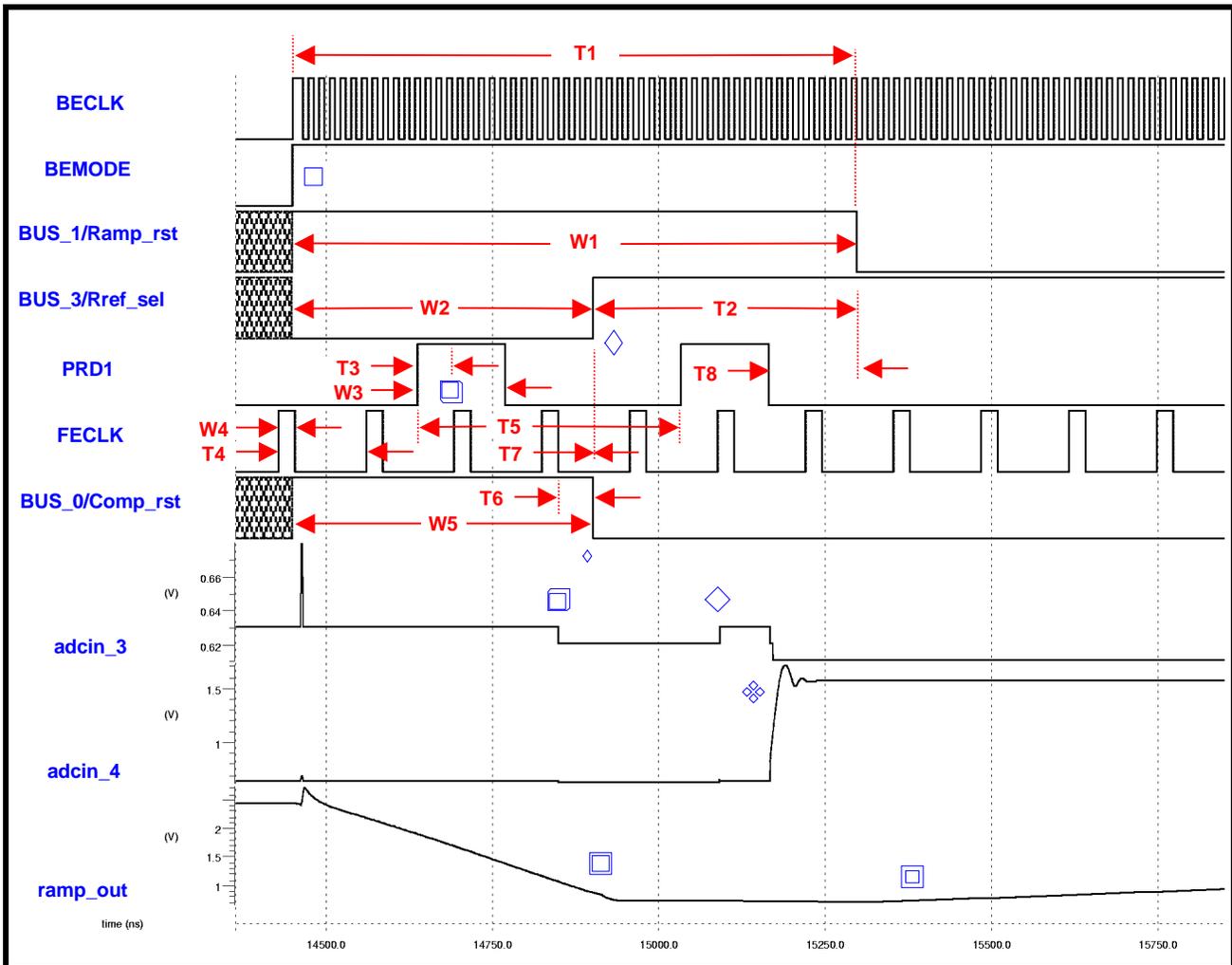


I. Pipeline Read/ADC Timing



Timing Spec	Description	Min	Nom	Max
adc.T1	1 st - BECLK to $\bar{\text{Ramp_rst}}$	4* BECLK	900 nS	--
adc.W1	Width of Ramp_rst in DIGITIZE mode	600 nS	900 nS	--
adc.W2	Width of RRef_sel low under Ramp_rst	500 nS	600 nS	--
adc.T2	- RRef_sel to $\bar{\text{Ramp_rst}}$	200 nS	300 nS	--
adc.T3	- PRD1 to 1 st - FECLK of pipeline read	5 nS	54 nS	--
adc.W3	Width of a PRD1	30 nS	1* FECLK	--
adc.W4	Width of FECLK high	20 nS	25 nS	--
adc.T4	Period of FECLK	65 nS	132 nS	--
adc.T5	Time between two - PRD1 for pipeline read	3* FECLK	4* FECLK	--
adc.T6	2 nd - FECLK of pipeline read to $\bar{\text{Comp_rst}}$	55 nS	132 nS	--
adc.T7	$\bar{\text{Comp_rst}}$ to - RRef_sel	50 nS	50 nS	--
adc.W5	Width of Comp_rst	100 nS	455 nS	--
adc.T8	2 nd - PRD1 to $\bar{\text{Ramp_rst}}$	100 nS	132 nS	--

PRD/ADC Timing Explained

The pipeline read/ADC timing consists of two sets of interdependent signal sequences. One is the *ADC Ramp Setup* (**BECLK/Ramp_rst/Rref_sel**), and the other *Pipeline Read* (**PRD1/FECLK/Comp_rst**). The *ADC Ramp Setup* controls the ADC ramp generator, the selection of the ADC ramp reference voltage (fixed) or the ADC ramp pedestal (programmable), and start of the ADC counter when not in Real-Time Pedestal Subtraction mode (RTPS). The *Pipeline Read* sequence controls the signal/pedestal CDS of the pipeline read amplifier on one terminal of the ADC input comparator, as well as the ADC ramp sampling on the other. Significant features of the sequences are described below.

ADC Ramp Setup

- 1) Pipeline read and signal digitization is initiated by entering DIGITIZE mode, that is, by asserting (**FEMODE=1 + BEMODE=1**) under **CHMODE=1** [□]. If **CHMODE=0**, DIGITIZE will instead be entered at **-CHMODE** when (**FEMODE=1 + BEMODE=1**). This behavior is the result of the MODE pins being processed through a transparent D-latch, which is controlled by **CHMODE**. MODE changes must occur on or about **-BECLK**, or while **BECLK=0**. Upon entering DIGITIZE, the I/O pins **BUS_0**, **BUS_1**, **BUS_3**, change function to **Comp_rst**, **Ramp_rst**, **RRef_sel**, respectively.
- 2) Asserting **RRef_sel=0** while **Ramp_rst=1** resets the ADC ramp to the fixed ADC ramp reference voltage level [□], which is above the programmable ramp pedestal voltage level. **RRef_sel=0** while **Ramp_rst=1** must then be asserted in concert with **Comp_rst**, as described below, in order to subtract the programmed pedestal value from the ramp reference voltage. Asserting **Ramp_rst=1** also asserts the internal counter reset signal **Cntr_Rst** when RTPS mode is off.
- 3) When **Ramp_rst** is de-asserted the ADC ramp commences in the programmed direction [□]. If RTPS mode is off, the internal signal **Cntr_Rst** will also be de-asserted. If RTPS mode is selected, **Cntr_Rst** is controlled by the dynamic threshold comparator circuit. In this case, the counter will be held in reset until the dynamic threshold comparator fires, sometime after the ADC ramp is initiated.

Pipeline Read

- 4) The pipeline signal/pedestal sampling sequence is initiated by **-FECLK** under **PRD1=1**. The relationship of **PRD1** and **FECLK** is fixed in terms of the state of **PRD1** during the phases of **FECLK**, as specified above. The 1st **-FECLK** under **PRD1** begins the cycle [□]. In the above example, the programmed order (“PB” config bit) is pedestal/signal.
- 5) During time **adc.T6**, the pipeline pedestal values are sampled onto the ADC input capacitors while the ADC comparator inputs (the other terminal of the input capacitors) are reset to a fixed internal reference level. Concurrently, during time **adc.W5** the ramp reference level is being sampled onto identical comparator input capacitors on the other comparator input terminal. It can be seen on the internal

signal **adcin_3** (no-hit channel) that the pipeline pedestal value is available to the ADC at the 2nd **FECLK** [□].

- 6) When **Comp_rst** is de-asserted the ADC comparators are un-reset [◇]. The ADC input sampling capacitors are now pre-charged to the pipeline pedestal values. From this time on, the ADC input is reading the difference of the pipeline output and the sampled pipeline pedestal, thus the CDS cycle is complete. However, the correct pipeline signal value will not be applied until the 2nd **PRD1**.
- 7) - **RRef_sel** applies the desired offset to the other ADC comparator input capacitor [◇]. This action must take place after **Comp_rst** (**adc.T7**) in order to achieve the desired CDS operation (rampref-ramped) on the ramp. Note that the effect of this CDS operation is to pre-charge a small offset across the ramp capacitor, which the ramp must “make-up” before it achieves zero-crossing of the original ramp reference level value. The purpose of this process is to allow the ramp to slew for a small period into its linear region, so that the ADC comparators will fire within the linear region of the ramp for small input signals. This is especially important for accurate noise measurement.
- 8) On the 3rd **FECLK**, under the 2nd **PRD1**=1, the pipeline pedestal value is de-asserted by the pipeline read amp [◇]. On the 2nd **PRD1** the signal values are asserted by the pipeline read amp [✦] *{I am not sure if this is correct—the simulation shows this is the case, but Tom’s measurements on the pipeline test chip indicate that it comes on falling FECLK just like the pedestal values—Brad}*. This can be clearly seen on the internal signal **adcin_4** (hit channel) above. Time **adc.T8** is required to allow the pipeline read amp to settle (and hence the signal-pedestal value at the ADC input) before starting the conversion.