Chips for Prototyping

We used up ~ 100 good dies already for chip testing and hybrid prototypes.

Taking into account the 6-in run problem, we should probably be more careful with die usage. Possible prototyping solutions:

- Use SVX3D radsoft chips from HP. We still have 3 more wafers from the prototype SVX3D run. Taking yield into account, this is ~ 200 chips. Known problems: pedestal overshoot in the first 5 channels, the dynamic common mode noise suppression circuitry doesn't work.

- There are 17 useable dies on the wafer which haven't been backgrinded and backplated.

- Use fair dies, not good ones.

- Reclassify bad dies.