Testing Front-End Electronics for the CDF Silicon Upgrade

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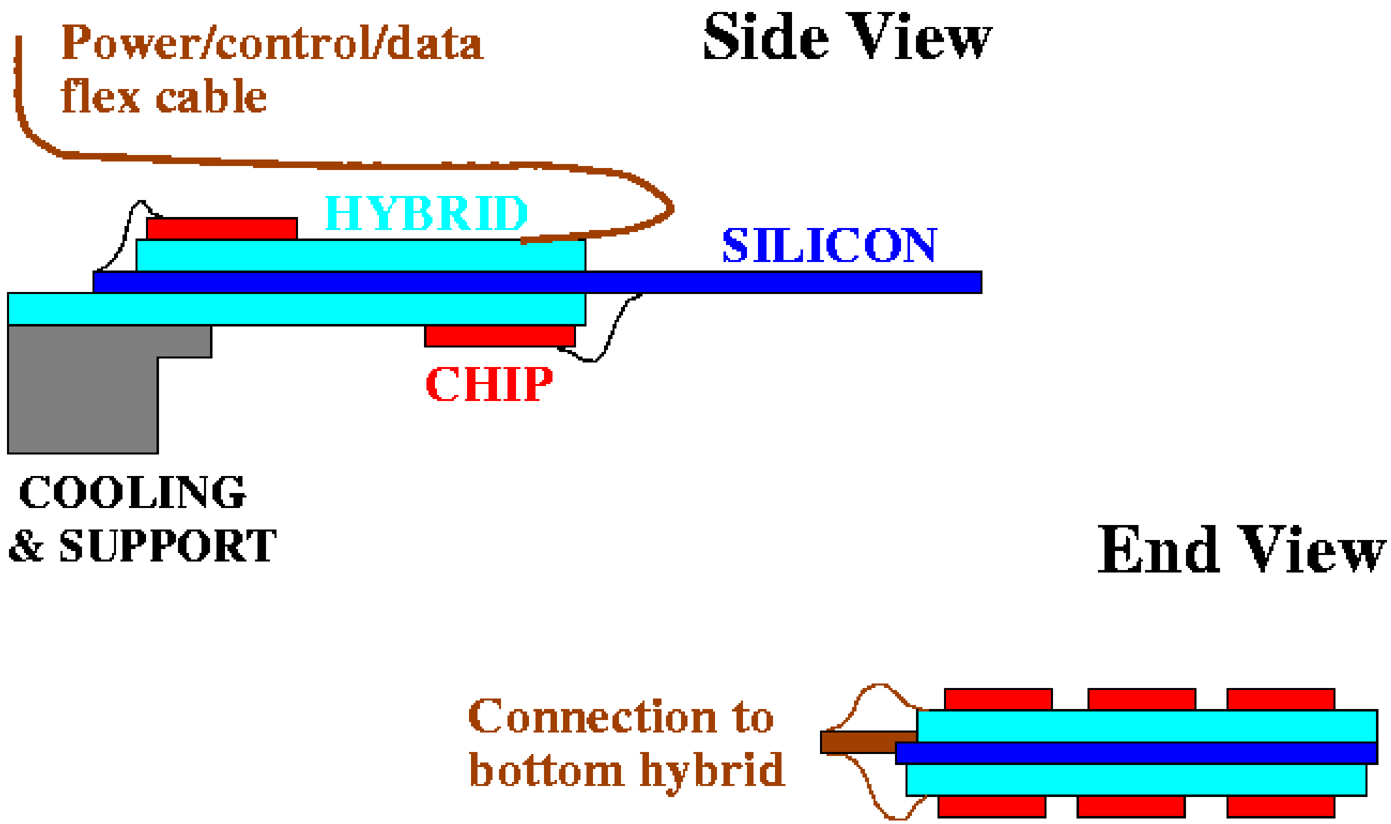
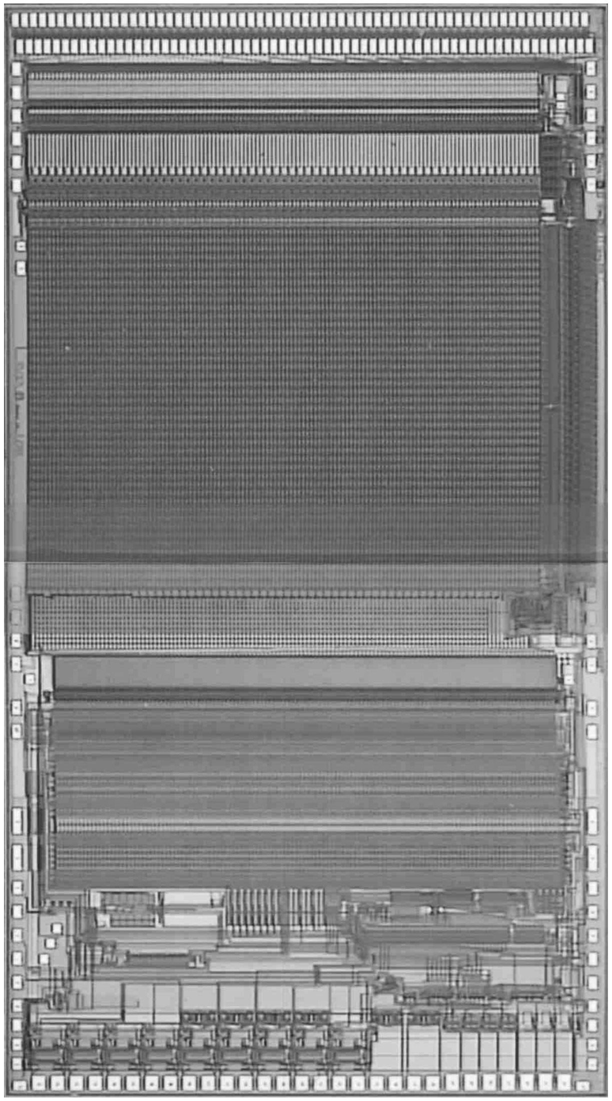
SVXII Ladder Schematic



SVX3D ASIC



- 128 input channels
- Designed to operate with 132 or 396 ns beam crossing rate
- ENC = 700 + 53 electrons/pF
- 46 cell analog pipeline
- Buffers up to 4 events
- 8-bit Wilkinson ADC, digital readout
- Deadtimeless operation
- On-chip sparsification and common mode noise suppression
- Fabricated in the Honeywell 0.8μm radiation hard process

- Modern HEP experiments rely on ASICs for high channel count data acquisition
- VLSI IC design is not a common skill among particle physicists... but we can help with
  - design specifications
  - circuit ideas
  - project management
  - testing and quality control
- Tight collaboration between physicists and IC designers is essential for success

Taxonomy of IC Testing

- Design verification
  - This is the initial phase in which tests are performed on prototype chips to ensure that the circuit implements what it is supposed to do AND does not have any unexpected "features"
- Reliability studies
  - Small samples of parts are operated during radiation exposures and/or at elevated temperatures
- Production testing
  - Ensures that only defect-free parts are used in subsequent stages of detector construction

SVX3D Testing Challenges

- Complex mixed-signal ASIC
- Must verify radiation hardness
- Moderate part count
  - Too large for a generic test setup
  - Too small to buy industrial-strength ATE
- Many failure modes, relatively low yield
- Tight budget

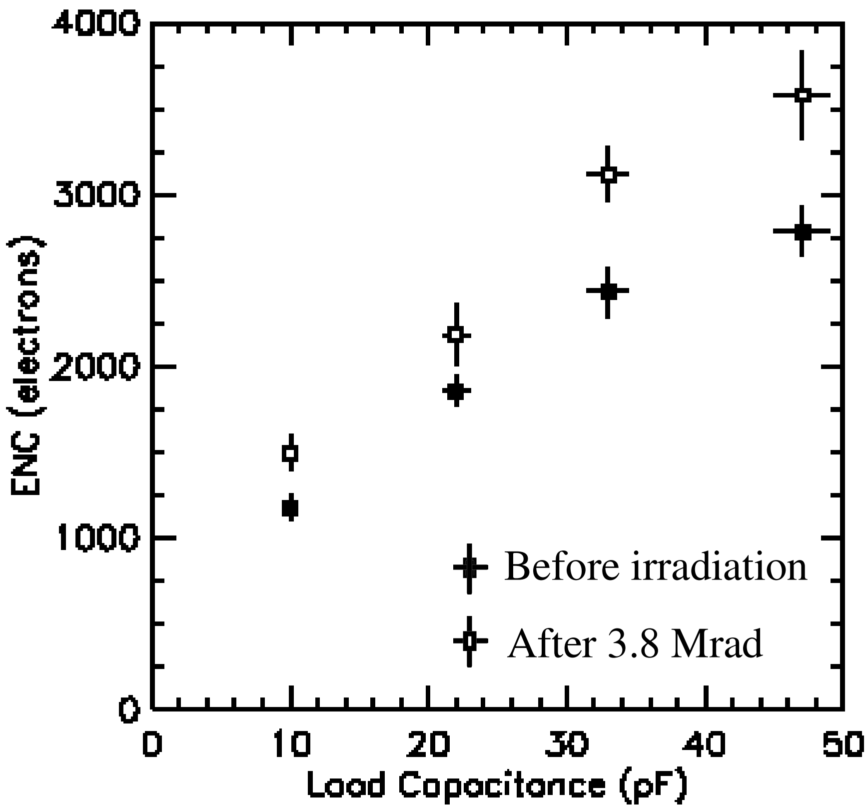
Basic Test Setup

- Custom-built pattern generator/readout board
  - Pattern and readout FIFOs with clock, parallel I/O, and glue logic. Runs continuously or from external trigger.
- Level shifter and device adapters
- Programmable power supply with GPIB
- Linux PC with several add-on cards:
  - Keithley KPCI-PIO96 digital I/O card
  - ComputerBoards CIO-DAC02/16 analog output card
  - National Instruments PCI-GPIB controller
- Test software

Software Design

- Open source software has been used with great success throughout the whole project:
  - Database engine: Berkeley DB
  - Data visualization: Histo-Scope, BLT, FIG
  - Data analysis: Histo-Scope, CERNLIB
  - Report generation: LaTeX
  - GUI tools: Tcl/Tk and various Tcl extensions
  - Overall glue: Tcl, C code
- Special attention has been given to data visualization and presentation of results

Radiation Testing

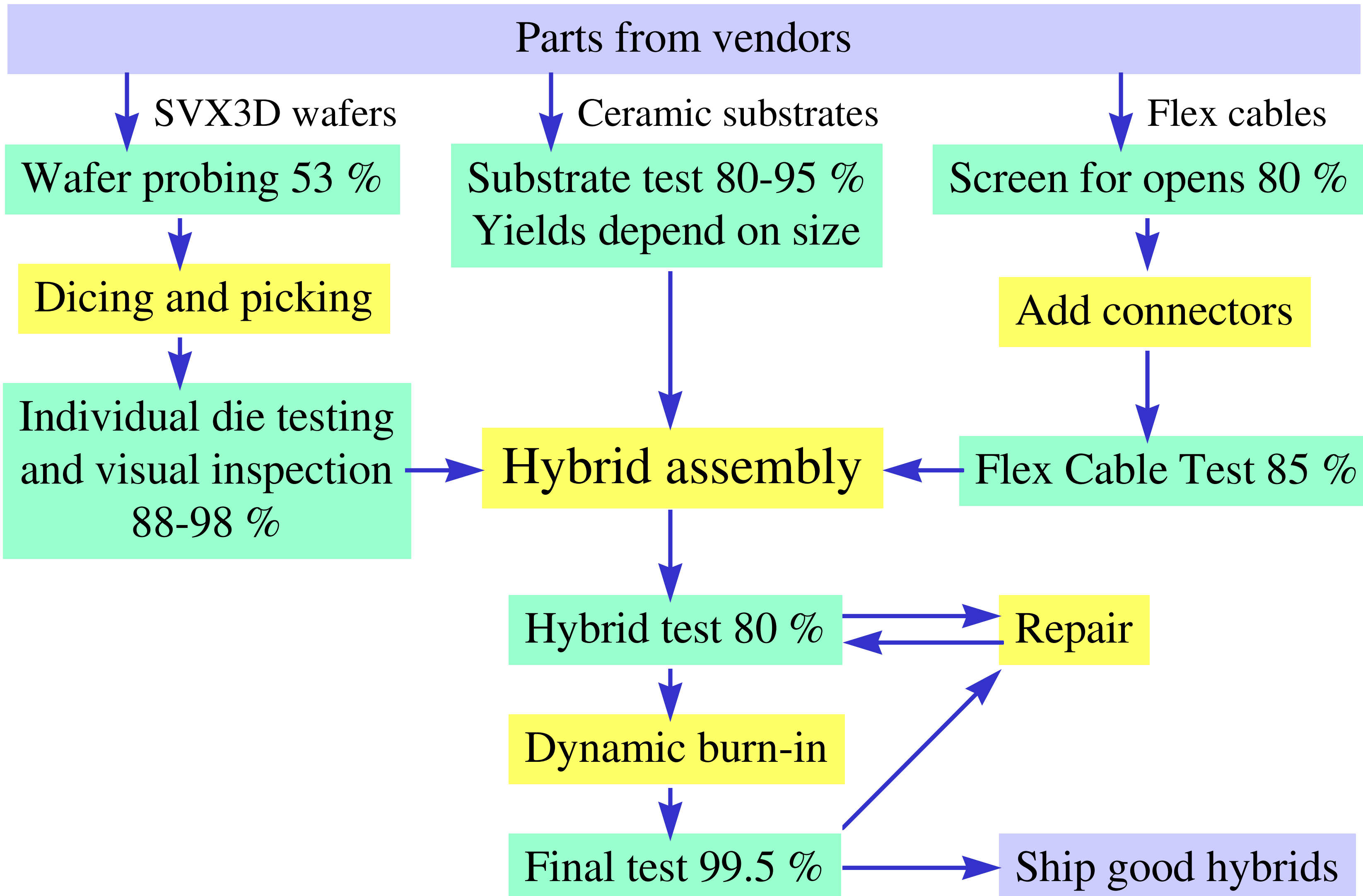


- Chip performance has been verified up to 4 Mrad
- At 2 Mrad (max. dose for sensors) chip noise increases by ~ 20%
- Consistent results from both ^{60}Co γ source and 55 MeV proton beam

SVX3D Production Testing Strategy

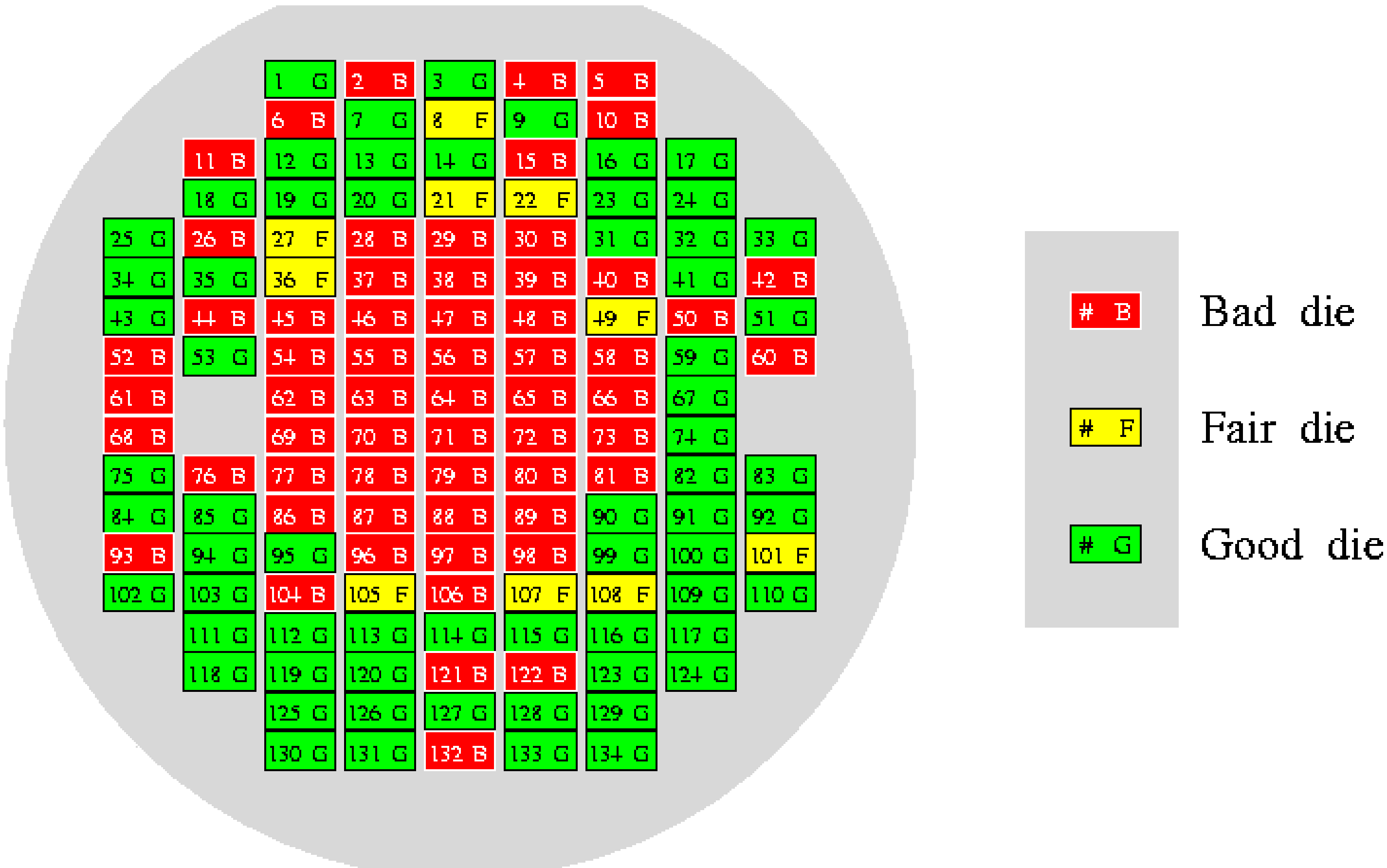
- Speed is not critical – carry out exhaustive checks of all specifications. Exercise all features and scan all operating parameters.
  - No reliable fault models were available when the testing started
- Sequence tests from “easy” to “hard”.
  - Check voltages and currents
  - Test digital logic
  - Characterize analog performance
- Save test data. Refine the analysis when more information about failure modes is accumulated.

Hybrid Production Testing and Yields



Die quality map for wafer 186 s/n: Y21316-09-15

Date: 07/13/99



Summary

- A successful testing program for silicon readout ASICs and hybrids has been developed at LBNL to complement IC design and hybrid production efforts
- The SVX3D chip performance has been studied in a wide range of operation conditions and absorbed doses
- Tested more than 20,000 chips and 1,700 hybrids
- This experience is relevant for future HEP experiments