Testing of readout electronics for the Silicon Vertex Tracker of the Collider Detector at Fermilab

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May 20, 1998

Contents

Chapter 1

The Collider Detector at the Fermilab and Top quark physics

In this chapter, we give a short description of the Collider Detector at the Fermilab (CDF) and the physics behind.

1.1 The Standard Model and the discovery of the Top Quark

1.1.1 The Standard Model

The standard model is the theoretical picture of how elementary particles are organized and how they interact with one another via the forces.

According to this picture, matter consists of two types of particles: ***quarks*** and ***leptons***. These are associated into generations. There are six quarks (up, down, strange, charm, bottom and top) and six leptons (electron, muon, tau and a neutrino associated with each of the three).

Up and down quarks occur along with electrons inside atoms; they are members of the first generation. Much heavier quarks such as the top and bottom are created only in accelerators. For each quark or lepton, there is an antiquark or antilepton with opposite charge. Quarks can only be observed in bound states called hadrons.

Force is transmitted by a different set of particles: photons, gluons, Z and W, known generically as ***bosons***. The photon transmits the electromagnetic force which at high energies is unified with the weak force. The gluons transmit the strong force. The W and Z bosons transmit the weak nuclear force. An up quark may, for example, change into a down quark by emitting a W particle.

Particles	First generation	Second generation	Third generation
Quarks	Up, u	Charm, c	Top, t
	0.3GeV	1.5GeV	176GeV
	Down, d	Strange, s	Bottom, b
	0.3GeV	0.5 GeV	4.5 GeV
Leptons	Electron, e^-	Muon, μ^-	Tau, τ^-
	0.0005 GeV	0.106 GeV	1.7 GeV
	ν_e	ν_μ	ν_τ
	0? GeV	0? GeV	0? GeV

Table 1.1: *Elementary particles, their symbols and their masses.*

Transmitters of force	Vector bosons	Photons	Gluon
Symbol	W^+, W^-, Z^0	γ	g
Force	WEAK	Electromagnetic	Strong

Table 1.2: *Transmitters of force and the forces they convey.*

1.1.2 Discovery of the Top Quark

In may 1995 the existence of the long sought top quark, the last of the six quarks required by the standard model, was established using data samples collected by the Collider Detector at Fermilab (CDF). The discovery is considered as an important confirmation of the validity of the standard model.

The top quarks were produced in the $\bar{p}p$ (proton-antiproton) collider at Fermilab. Measurements are obstructed by background phenomenas, but thanks to b-tagging in the Silicon VerteX (SVX) tracker of the CDF (see following section about detecting particles), a clear excess of signal over background was found.

The mass of the top quark was measured to be $176 \pm 8 \pm 10 GeV/c^2$.

1.2 Producing Top Quarks - the Tevatron at Fermilab

1.2.1 Top Quark production

The top quark observed so far at Fermilab have all been created through the reaction

$$p\bar{p} \longrightarrow t + \bar{t} + hadrons$$

Highly energetic bunches of protons and antiprotons are made to collide head on, in some cases producing a top, an antitop and jets of hadrons. However the production rate is extreemely small compared with that of other processes. During the first measurements, 12 relevant events were isolated from the trillion or so collisions. Also the total center of mass needed to produce a top-antitop pair is very important due to the high mass of the top quark. The tevatron at Fermilab was the first collider to reach sufficiently high energies for the observation of the top quark.

1.2.2 The Tevatron at Fermilab

With a combination of linear and circular accelerators the accelerator complex at the Enrico Fermi National Laboratories (FNAL), is still world leading when it comes to creating beams of high-energy protons and antiprotons. The most powerful accelerator is known as the Tevatron because of its ability to accelerate protons to nearly one trillion electron volts ($1TeV$). It is a synchrotron and uses cavities in which a radio-frequency wave is injected to accelerate the particles. The part of this wave closest to the beam has an electric field aligned so that the charged particle gets a boost in the right direction at that time.

Accelerated particles gather in bunches. When there are six bunches each of protons and anti-protons they will collide at six different locations along the Tevatron ring: these are potential emplacements for particle detectors.

1.3 Detecting the Top Quark - the Collider Detector at Fermilab

1.3.1 Top decay

The top quark has a lifetime of 10^{-24} second. It decays almost instantly. According to the Standard Model described above, this decay will almost always produce a W and a bottom quark.

Unfortunately, neither can be directly observed. The lifetime of the W is close to that of the top. The bottom quark is also very unstable, though much longer lived with than the top. Moreover, the strong force [1] ensures that quarks are never observed individually. They always occur together with other quarks as hadrons. "When a quark emerges from a collision, it gets dressed up by a cloud of other quarks and antiquarks. What is observed is a jet, a directed beam of particles that have roughly the same direction as the original quark."([6]).

The W has two mechanisms of decay:

- into two quarks from the same generation, and the result of the top decay can be written as:

$$t \longrightarrow 3jets \; ; \; \bar{t} \longrightarrow 3jets$$

- into a lepton and a lepton neutrino from the same generation.

$$t \longrightarrow l^+ + \nu_l + jet \; ; \; \bar{t} \longrightarrow l^- + \bar{\nu_l} + jet$$

[1] The strong force binds quarks together. See the description of the Standard Model.

1.3.2 The Collider Detector at Fermilab (CDF)

Figure 1.1: *An elevation view of the Collider Detector at Fermilab (CDF) showing the different detecting components. Figure 2.1 shows an enlargement of the three barrels of the central Silicon VerteX tracker (SVXII).*

A schematic elevation view of the upgraded version of the Collider Detector at Fermilab, that first observed the top quark, is shown in figure 1.1. CDF is one of two particle detectors located along the Tevatron collider, mentioned in previous section (the other one being the D0 detector). It is a solenoidal detector which combines precision charged particle tracking with fast projective calorimetry and fine grained muon detection.

Tracking systems

The tracking systems are mainly used to reconstruct tracks of charged particles traversing them, thus allowing singeling out of relevant events. They consist of three detecting elements contained in a superconducting solenoid generating a 1.4 Tesla magnetic field parallel to the beam axis. Starting from the inside:

- The Silicon VerteX Detector (SVX), decribed in detail in next chapter.
- The Intermediary Silicon Layers (ISL), using the same technology as the SVX but with a different geometry. ISL and SVX work as a unit.
- The Central Outer Tracker, a driftwire chamber that tracks charged particles through a system of wire-shaped anodes collecting electrons released when the particles ionize a gas.

Calorimeters

Outside the solenoid, scintillator-based calorimetry [2] provides separate energy measurements for hadrons and electromagnetic particles.

Muon detectors

Four systems of scintillators and proportional chambers will be used in the detection of muons.

[2]in suitable materials, called *scintillators*, a fraction of the energy lost by traversing charged particles will reemerge as visible light. This light is multiplied by a photomultiplier and amplified to give an electronic pulse.

1.4 Run II and the upgrade of the CDF

1.4.1 Physics goals

Until the completion of the Large Hadron Collider (LHC) at CERN the Fermilab Tevatron Collider remains the high energy frontier of particle physics. The upgrade of the detectors will allow a program of precision hadron physics that will attack open questions from many complementary directions. Further characterization of the properties of the Top Quark will be an important part of this program that will also be devoted to electroweak physics and the direct search for new phenomenas.

The new set of experiments, commonly referred to as RunII, will benefit from a slight increase in total center of mass energy (reaching $2TeV$), an increase in luminosity (up to 2×10^{32}) and a decrease in the time between crossings (two crossing times are discussed: $132ns$ and $396ns$).

1.4.2 Upgrades and new requirements

The description in following chapters focuses exclusively over the upgraded version of the CDF detector, commonly referred to as the CDFII.

The increase in energy will increase the $t\bar{t}$ yield by 40%. Detector issues are however mostly driven by the luminosity, the number of bunches and the time between beamcrossings. Much of the CDF upgrade is necessitated by the new time structure (more collisions in less time).

The electronics systems must be substantially altered. The increased instantaneous luminosity requires a similar increase in data transfer rates. It is however the reduced spacing between accelerator bunches that has the greatest impact, necessecitating a new architecture for the readout system.

Another challenging new design goal is the deadtimeless architecture. In previous runs, datacollection had to be halted during readout. The wish is that the new detector should suffer from as little dead time as possible.

Chapter 2

The Silicon Vertex Detector

2.1 General purpose and description

2.1.1 Vertex detection using silicon sensors

The need for very high spatial precision

The use of semiconductors for position measurement in particle physics stems from the extreme precision needed for the measurement of very rare and very short lived particles such as tau leptons, charmed particles and bottom particles.

These particles have lifetimes of the order of a picosecond. They are created at point called the primary vertex by a high energy collision. After traveling a short distance they will decay into several other particles at a secondary vertex. The order of the distance between primary and secondary vertex is given by:

$$dx = \text{lifetime} * c$$

Detectors with a higher precision than this distance must be used in order to distinguish primary and secondary vertices.

Tracking with silicon detectors

Vertices are found by reconstructing the trajectories of the charged particles emerging from a collision with a set of detectors arranged near the point where the collision takes place.

A microstrip detector can be visualized as a large number of thin strip-shaped diodes on a silicon wafer. Each strip is connected to a separate electronic readout channel and should give a signal only if an ionizing particle "hits" or traverses the detector in a region close to the strip. The location of the strip being hit yields two coordinates [1] (for example r and ϕ). The remaining coordinate (in this case z) can be determined by using other silicon detectors with a different

[1] The polar angle θ is measured from the proton direction, the azimuthal angle ϕ is measured from the Tevatron plane, and the pseudo-rapidity is defined as $\eta = -ln\left(tan\frac{\theta}{2}\right)$

strip orientation, or can be negelected, permitting the reconstruction of vertices in only two dimensions. Double sided detectors have segmented outputs on both sides of the same silicon wafer and thus a single sensor can produce a three-coordinate measurement. This kind of detectors will be used in the SVXII tracker.

The trajectory of a charged particle can be reconstructed by combining data from several layers of silicon sensors. The result of the reconstruction is known as a ***track***. In the SVXII, 5 concentric layers of silicon microstrip detectors help find the tracks of the various ionizing particles. Complementary information is also provided by three additional layers of silicon (ISL) and a drift-wire chamber located outside the silicon vertex detector (See the description of the CDFII detector in chapter 1).

The reconstructed tracks are extrapolated back to the vicinity of the primary vertex. The trajectories of the particles arising from the decay of a long-lived particle converge at a secondary vertex that, if all goes well, is resolved from the primary vertex.

2.1.2 General description of the SVXII Detector

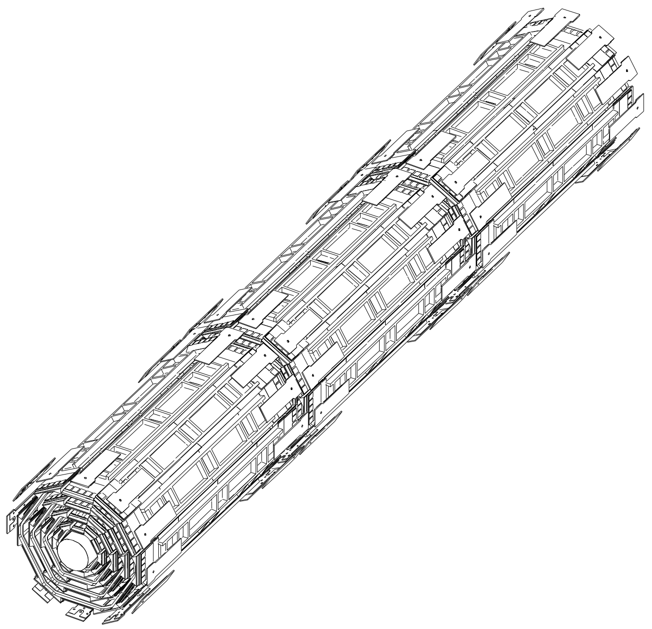

Figure 2.1: ***The three barrels of the Silicon VerteX detector, the innermost tracker of the CDF detector. 720 microstrip sensors are arranged in five cocentric cylindrical layers totaling 405 000 electronic readout channels.***

The upgrade of the Silicon Vertex Detector that will be used for the Run II CDF experiment is denominated the SVXII. It will use 720 double-sided, $7.4cm$ long silicon sensors arranged on 5 coaxial cylinders (***layers***). (fig. 2.1). The different layers are numbered from level 0 to level 4, level 0 being the layer closest to the beam.

A ladder is a unit consisting of two pairs of wire-bonded detectors and, on each side of the end detector, a beryllia ceramic hybrid supporting a number of readout chips.

Ladders will be held in 5-layer ***barrel*** structures with 12 ladders per layer. Each barrel will have two beryllium bulkheads for mechanical support and electronics cooling. There will be 3 barrels combined end-to-end for a total length of $87cm$.

The number of ladders is the same for each layer and the length is the same for all ladders but the width of the the ladders varies from one layer to another.

2.2 The Silicon Microstrip Sensors

2.2.1 Detecting ionizing particles with a silicon sensor

Strip detectors

A strip detector consists of a large number of strip-shaped implants of a heavy dopant concentration on an oppositely doped silicon wafer. The interface between doped implant and bulk silicon is called ***pn-junction*** [2]. When subject to a suitable voltage drop, a region around the interface will be depleted of charge carriers. This region is referred to as the ***depleted region.*** Electrically it is an effective vacuum with an electric field.

Importance of the depleted region

Charged particles are detected through the charge carrier pairs they create when traversing the depleted region of the sensors [3]. The depleted region is the active area of the detector and the strive is to make it as thick as possible. The thickness of the depleted region varies with the applied voltage (fig. 2.2) as

$$W = \sqrt{\frac{2\epsilon(V+V_{bi})}{ne}} = \sqrt{2\rho\mu\epsilon}$$

[2] See Appendix A for further details about semiconductors and junctions.

[3] See following section.

where

V	$=$	external bias voltage
V_{bi}	$=$	"built-in" voltage ($\approx 0.8V$ for most detectors)
n	$=$	doping concentration
e	$=$	electron charge
ϵ	$=$	dielectric constant $= 11.9\epsilon_0 \approx 1pF/cm$
ρ	$=$	resistivity (typically $1 - 10k\Omega cm$)
μ	$=$	charge carrier mobility
		$= 1350cm^2V^{-1}s^{-1}$ for electrons
		$= 450cm^2V^{-1}s^{-1}$ for holes

or

$$W = 0.5\mu m \times \sqrt{\rho(V+V_{bi})} \text{ for } n\text{-type material}$$

and

$$W = 0.3\mu m \times \sqrt{\rho(V+V_{bi})} \text{ for } p\text{-type material}$$

Full depletion is reached when the depleted region covers all the bulk silicon.

The entire design of the silicon sensor aims at giving the depleted region an optimal extension and shape.

Electron-hole pair production

When a minimum-ionizing particle (mip) hits the depleted region electron-hole pairs are created (fig. 2.3). The generated pairs will be separated by the electric

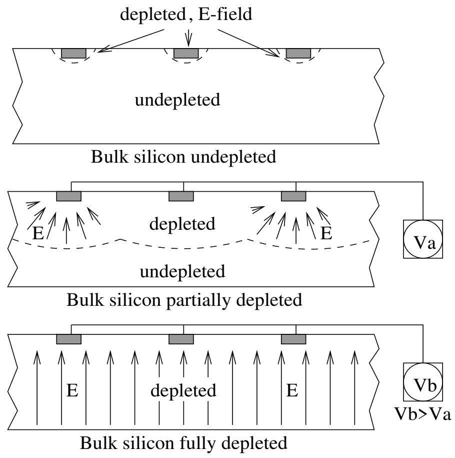

Figure 2.2: *Schematic view of the depletion process: non depleted, partially depleted and fully depleted. Around the pn-junction, a thin area is depleted of charege carriers, allowing the build up of an electric field (top figure). When a voltage is applied across the junction, the depleted region expands (middle figure) until full depletion is reached (lower figure).*

field and drawn to the electrodes. Electrons are drawn to the p-side of the detector while holes go to the n-side.

The mean energy deposited by a minimum-ionizing particle traversing a $300\mu m$ sensor is around $50keV$. Electrons are promoted across the band gap to generate charge carriers in the depleted bulk. The band gap is $1.1eV$ but, because of the energy distribution of the electrons, the energy needed to generate a pair of charge carriers will, on average, be higher than this. A deposited energy of $50keV$ corresponds to approximately 24000 electron-hole pairs being generated.

The thickness of a silicon sensor is invaryably $300\mu m$. The amount of energy deposited by a charged particle traversing the detector is proportional to the length it travels in the depleted silicon and thus proportional to the thickness of the sensor. However recombination processes in the silicon limit the lifetime of an electron-hole pair. The speed of the charge carriers is also limited in silicon and the optimal thickness of a silicon detector is found to be:

$$Thickness = speed\ of\ charge\ carriers \times mean\ lifetime\ of\ charge\ carriers$$

The charge concentration is modified locally at the p^+n-junction, but only briefly. As the implants are connected via bias resistors to voltage sources, a current will flow in the strip. A MOS-junction assures a capacitive coupling to metal strips on top of the p^+- and n-strips that transmit a current pulse to the readoutchip.

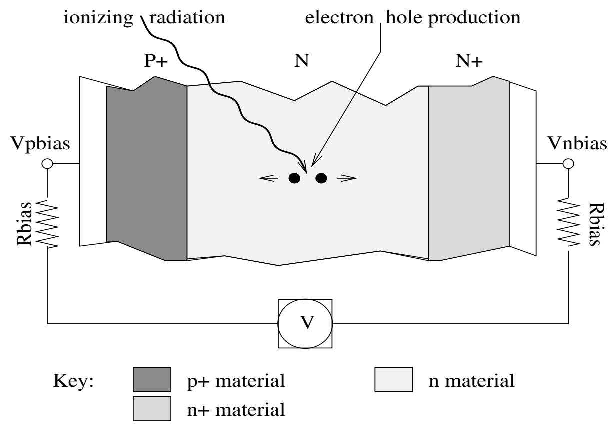

Figure 2.3: *Electron-hole production. When a sufficiently energetic ionizing particle traverses the microstrip sensor some energy is used to create electron-hole pairs. These charge carriers are separated by the electric field (see figure 2.2) and migrate to each side of the sensor.*

Properties	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
number of ϕ strips	256	384	640	768	896
number of Z strips	256	576	640	512	896
stereo angle	$90°$	$90°$	$+1.2°$	$90°$	$-1.2°$
ϕ strip pitch (μm)	60	62	60	60	65
Z strip pitch (μm)	141	125.5	60	141	65
Active width (mm)	15.300	23.746	38.340	46.020	58.175
Active length (mm)	72.43	72.43	72.43	72.43	72.43
Number of detectors	144	144	144	144	144

Table 2.1: ***Key data for the different layers: number of strips, pitch, width and length***

2.2.2 The SVXII sensors

Sensor layout

The SVXII has five layers of sensors. The sensors are all double-sided but differ from one layer to another when it comes to the width, the number of strips on the p-n junction side and the layout of the n side. Characteristics for the different layers are given in table below.

Layers 0, 1 and 3 have $90°$ sensors. The sensors have strips running lenghtwise on the sensors $p-n$ junction side to measure the $r-\phi$ position of the particle, and strips running laterally on the ohmic contact side (n-side) to measure the $r-z$ position. Both sets of strips are read out from the end of the sensors. For the $r-z$ signals this requires an additional layer of metal traces running longitudinally and contacting the lateral $r-z$ strips through a $5\mu m$ insulating layer of SiO_2 by means of small "vias" (fig. 2.4).

The Layer 2 and Layer 4 sensors utilize "small angle" stereo for the sensor layout instead of the $90°$ layout.

The combination of different layouts has been optimized for pattern recognition through Monte Carlo studies.

2.3 The SVX3 Readout Hybrid

The SVX3 Readout Hybrid connects sensor strips, readout chips, power supplies and control channels. The design of the hybrid is a compromise between contradictory needs:

1. Good thermal performance to conduct away heat from the chips. Maximizing thermal performace would imply having a high ***mass*** (and a high thermal conductivity).

2. Good ***electrical shielding.*** Electrical shielding improves with the size and with the ***mass.***

3. Small scattering of particles going through. The scattering would increase with the mass and size.

The hybrid consists of 6 interconnected silver and gold ink layers separated by dielectric on top of a 95% beryllium oxide substrate (fig. 2.5). The ink is standard for applications that require wire bonding. Additionally there are palladium-god ink pads on the top layer to permit soldering of surface mount components.

The total thickness of the printed material is about $400\mu m$.

The hybrid includes a bonding pad field on one side to allow for the same hybrid to be used on the phi- and z-sides of a ladder.

$\phi - z$ interconnection is accomplished via a custom thin film jumper which is glued to the side of the ladder.

2.4 The Svx3 Readout Chip

The Svx3 readout chip is the latest in a series of prototypes brought forward by successive improvements of the original design.

A Svx3 chip consists of 128 electronic channels each reading out one of the silicon sensor's strips. As the number of strips on the detectors increases with the layer number so does the number of chips per layer.

The chip is responsible for collecting and amplifying incoming signals from the silicon detector's strips. Information is stored as charge in a pipeline. Upon request the chip will digitize the signal and transmit it for further analysis. This work is carried out in parallel for each electronic channel of the chip.

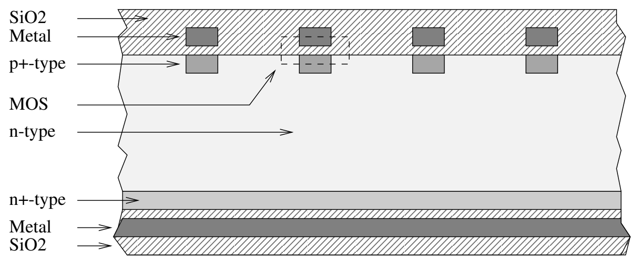

Figure 2.4: *Throughcut of a layer 0 SVXII silicon sensor. The beam axis is perpendicular to the picture. The upper half constitutes the p-side of the sensor with p^+ implants parallel to the beam axis. Metal strips connected to the readout electronics run on top of them. A thin layer of insulant (SiO_2) between strip and implant makes sure that they are AC-coupled (MOS-junction). The n-side doesn't have a pn-junction but serves as a charge collector. The n^+ implants are perpendicular to the p^+ implants and are also AC-coupled to readout electronics via MOS-junctions and two perpendicular layers of metal strips, schematically represented as one on the figure.*

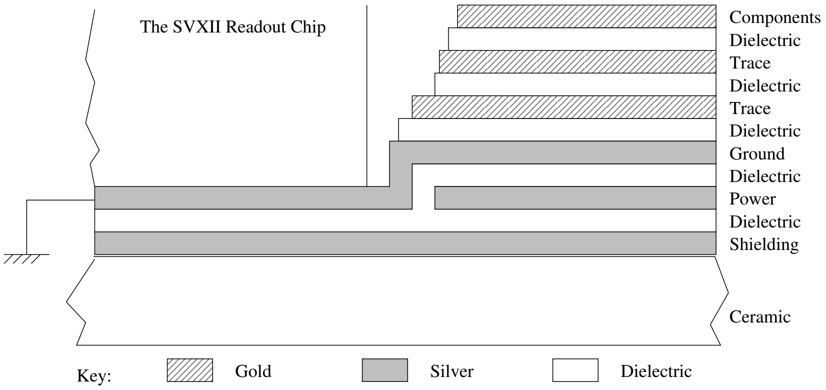

Figure 2.5: *Schematic over the different layers of the SVX3 Readout Hybrid that connects sensor strips, readout chips, power supplies and control channels. It consists of 6 interconnected silver and gold ink layers separated by dielectric on top of a 95% beryllium oxide substrate.*

Layer	0	1	2	3	4
# of chips per ladder, ϕ-side	2	3	5	6	7
# of chips per ladder, Z-side	2	3	5	4	7

Table 2.2: Number of chips per layer and side.

Earlier prototypes of the readout chip were divided in a ***Front End*** chip end a ***Back End*** chip wire bonded together. The Svx3d version of the chip is monolithic but still has the same basic features as earlier prototypes.

2.4.1 Front End - Amplification and Pipeline

The Preamplifier

The first key element of the Front End is a charge integrating amplifier with a capacitive feedback loop between inverting input and output (fig. 2.6). It is commonly referred to as the Preamplifier. The feedback capacitance is $0.2pF$ and thus the gain of the Preamplifier is $5mV/fC$.

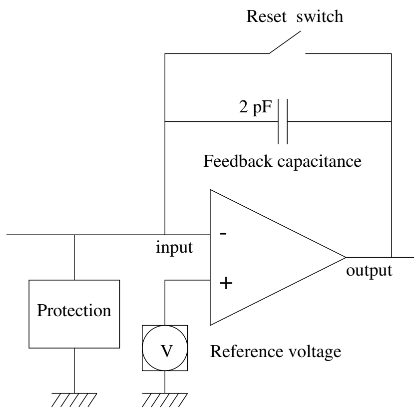

Figure 2.6: ***The Preamplifier, protection circuit and feed back loop.***

When charge is presented at its input, the Preamplifier will adjust the output voltage in order to collect the charge across the feedback capacitance, thus maintaining the input voltage constant. However the output voltage is only allowed to vary within the dynamic range which, for the Svx3, spans 0.7 to $4.2V$ which corresponds to a collected charge of $450fC$. When the limits of the dynamic range are reached, the Preamplifier will cease to respond to incoming signals and is said to be saturated.

The charge integrator has an adjustable bandwidth for 10-90% rise times from $60ns$ to $240ns$ with 10 to $30pF$ loads.

The Preamplifier can be reset by closing a reset switch. The feedback capacitance will then discharge, and the output voltage will return to a fixed reference value. Full reset and settling takes $1.6\mu s$ but the full dynamic range allows continuous operation over many beam crossings.

A protection device limits the voltage at the input to protect the readout chip in the event of a broken MOS-capacitance on the sensor.

The Pipeline

For each beam crossing, the charge integrated over the Preamplifier's feedback capacitance between this beam crossing and the next is stored in a Pipeline. This Pipeline is also located in the Front End and consists of a switched array of 47 capacitors, each of which can be placed in a capacitive loop with one of two voltage amplifiers: the read (R) and write (W) amplifiers (fig. 2.7).

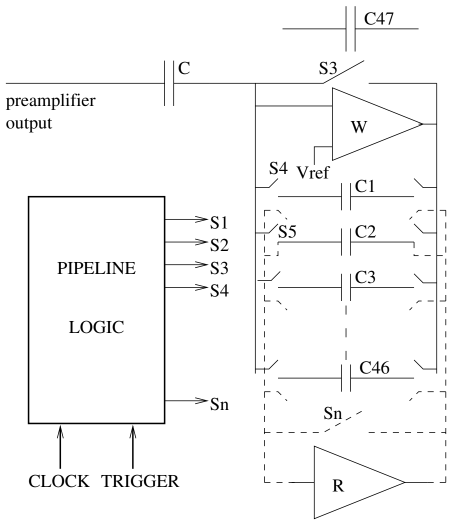

Figure 2.7: *The Pipeline.*

Writing on the pipeline

$25ns$ before every beam crossing, one of 46 "loop" capacitors is switched into the W circuit, which is immediately reset to have zero charge on the capacitor for the present integrator output. After a beam crossing any change in the integrator is amplified onto the W capacitor, which is then switched out and left to hold its charge.

The capacitors are often referred to as cells or buckets. The pipeline logic determines which cell is to be written on. It will loop sequentially over the 46 capacitors. The operations of the pipeline logic are timed by the Front End clock, a control signal to the chip, synchronized with the beam crossings. As each bucket registers and event in time, the pipeline can be said to have a memory of 46 beam crossings.

Reading from the pipline and deadtimelessness

One of the main features of the Svx3 chip is that it is ***deadtimeless***. That is to say that it can write on the pipeline and read from it simultaneously. In earlier versions of the chip there was only a single pipeline operational amplifier, so no writing could be done while data was being read out, which meant events were not being registered during readout.

Upon a trigger, the capacitor from d crossings before the trigger is taken out of the loop by the pipeline logic. The value of d, the ***pipelaine delay***, is programmable between 0 and 41 and should be chosen to match the trigger latency. Up to 4 capacitors can be out of the loop at any given time, and can remain out indefinitely.

Capacitors out of the loop can be swithed into the R circuit whenever the Back End is ready, after which they are returned to the loop.

The 47th capacitor is not a part of the loop. It can be placed in the W circuit whenever there is a break in acquisition, in order to acquire an empty sample or W amplifier pedestal. It is then placed in the R circuit after every R cycle as a reference in order to compensate for residual charges from switching.

2.4.2 Back End - Digitization and Readout

Digitization

Once a cell has been marked for readout, the analog signal stored over its capacitance can be digitized. The digitization sequence takes place in the Back End of the chip (fig. 2.8).

The conversion of the analog signal to digital data is done by a Wilkinson ADC, consisting of a voltage ramp(common to all channels), an eight-bit digital counter (common to all channels), and one comparator per channel.

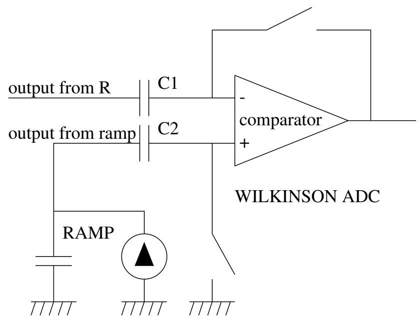

Figure 2.8: *Digitization.*

The ramp consists of an integrating circuit providing a fairly linear voltage increase for a short period of time.

The voltage from the operational amplifier R charges capacitor C_1 putting a voltage V_- over the comparator's inverting input. A double sampling technique is used so that V_- ends up being the difference in the output of R with

1. the capacitor cell selected by the trigger and
2. the 47^{th} pipeline capacitor

This voltage is proportional to the signal charge stored in the cell being read. The voltage V_+ over the non-inverting input is supplied by the voltage ramp and increases (or decreases, depending on ramp polarity) linearly with time. When V_+ crosses V_-, the comparator fires, switching the logic state of its output. The logic triggers a Flipflop latching the current value of the digital counter, common to all channels, in the particular channel's memory cell. The digital counter is synchronized with the radio frequency of the accelerator, i.e. $53MHz$. The counting rate is $106MHz$ because it counts on both edges of the clock.

The datastream

Data is output as a stream of 8 bit bytes. Bytes come in pairs, the first giving the channel number in binary code, the second providing the ADC information in gray code. [4]

Every time a new chip is read out the first byte will give the chip ID number and the following byte will be a pipeline cell number. The following stream gives the channel numbers and the read in information [5] in an ordered sequence.

2.4.3 Chip control

Initialisation

Chips on a same ladder are *daisy chained*. Each chip has two special pins, *top-* and *bottom-neighbour*.

During initialisation, information is provided to the chips as a chain of bits fed through the top neighbour of the first chip. For every new entry the chain advances one step. When it has gone through all cells of the first chip it goes out through the bottom neighbour and is passed on to the second chip through its top neighbour. In this way the same chain is fed through all the chips.

193 bits are used to initialize each chip. The first 128 bits are channel specific and determine the *calibration mask* of the chip. If bit i is high, charge can be injected in channel i. Whether charge is actually injected is determined in the pattern (see below) by a signal common to all channels.

The remaining 66 bits determine parameters common to all channels of the chip. These are:

- *Calibration polarity*: used to select the sign of the calibration charge pulse.
- *Pipeline and preamp polarity select*:
- *Preamp bandwidth*: changes the rise time of the Preamplifier.

[4] Every bitflip passing from one binary number to a consecutive one implies a voltage change which might induce pickup in the chip. Gray code is a way of rewriting binary numbers minimizing voltage changes.

[5] As the pairs mentioned above

- *Pipeline delay*: determines what cell in the pipeline should be read upon a trigger signal.
- *Pipeline read amplifier bias current*: adjusts various currents.
- *Pipeline polarity*: sets the order of pedestal-signal readout.
- *Chip ID*: sets th ID number of the chip. It will appear in the datastream.
- *Dynamic threshold*: subtracts the median of the pedestals to all channels for every cell in the pipeline.
- *Bias ratio select*: regulates the Back End current consumption.
- *Driver common mode select*: allows small shifts in the output logic level.
- *Last chip flag*: enabeled when the chip is the last in the daisy-chain.
- *Read neighbour bit*: if set to high, it will cause neighbouring channels to be read out along with a channel showing a hit.
- *Read all bit*: if set to high, it causes all channels of the chip to be read out upon a hit.
- *ADC ramp up/down*: determines the direction of the slope of the ADC ramp. Low equals down.
- *ADC comparator direction*: should be the same as the previous.
- *Ramp cap. adjust*: changes the ramp rate. Allows a maximum change of 10.
- *Sparsification threshold value*: sets the level of the sparsification threshold.
- *Counter modulo*: sets the maximum number that the counter counts to.
- *Ramp pedestal*: imposes a common offset to all channels.

Dynamic chip control

Continuous chip control is achieved by switching the logic states of a number of control signals. These signals reach all readout chips of the same side of a ladder via a cable connected to pads on the supporting hybrid. They determine the different functioning modes of the readout chips.

During readout a token called *priority* is passed from chip to chip to initiate readout.

Chapter 3

Ladder testing - theory and experimental setup

3.1 Experimental goals

3.1.1 Sparsification, pedestal and noise

The SVXII has 405504 readout channels. A complete readout of all channels would take $70\mu s$ which corresponds to a readout rate of around $10kHz$ with conventional techniques. This is far too slow for the new set of experiments the SVXII is being designed for. The desired peak readout rate is $50kHz$.

The need for higher readout rates has brought forward the concept of ***sparsification*** which aims at reading out only channels that show a hit. Calculations are based on an ***occupancy***, i.e. the percentage of channels hit, of less than 10%.

The main problem boils down to how to decide whether a channel has been hit or not. This leads us to the key concepts of noise and pedestal.

Even when a channel is not hit it will return a non-zero value, the ***pedestal***. For a given channel this pedestal has a gaussian distribution (fig. 3.1), the mean value of which represents the expected value of the channel without a hit, and the sigma represents the noise. In the Svx3 chip the pedestal can be adjusted by adding a common offset to all channels.

In order to be able to single out channels which have been hit one imposes a ***sparsification threshold*** common to all channels. Signals below this threshold will be discarded.

The level of the threshold is a compromise. It should be high enough to cut away undesired noise but at the same time it shouldn't prevent the detection of real signals. Too low a level would show false hits, known as ***noise occupancy***, and too high a level would substantially reduce the number of signals detected as these have a Landau distribution, implying a loss in efficiency.

3.1.2 Pedestal shifts and noise sources

Unfortunately pedestal values and noise can change from one channel to another and, for the same channel, with respect to time. These shifts affect both the width and the mean level of the pedestal, potentially leading to a broad non-gaussian pedestal distribution and thus increased noise occupancy. They are due to a variety of reasons and very often different phenomenas are interwoven.

1. Defects in the silicon sensors which can cause saturation of the Preamplifier. Through *capacitive coupling*, neighbouring channels can be affected.
2. *Deadtimeless operation*: fast asynchronous switching required for digitization and readout will induce noise onto sensitive analog functions of the Front End.
3. *Placing readout chips directly on active detector surfaces*: the sensor strips will pickup signals from chip, hybrid and cables.

The two latter are inherent to the new challenging design of the SVXII.

The hope is that a closer study and a better understanding of these phenomena will allow an optimisation of the threshold level and in some cases eleminate the causes or at least reduce the effects.

3.2 Pattern generation

3.2.1 Hardware

A scematic of the system used for testing chips mounted on testboards, hybrids and ladders is shown in figure 3.2.

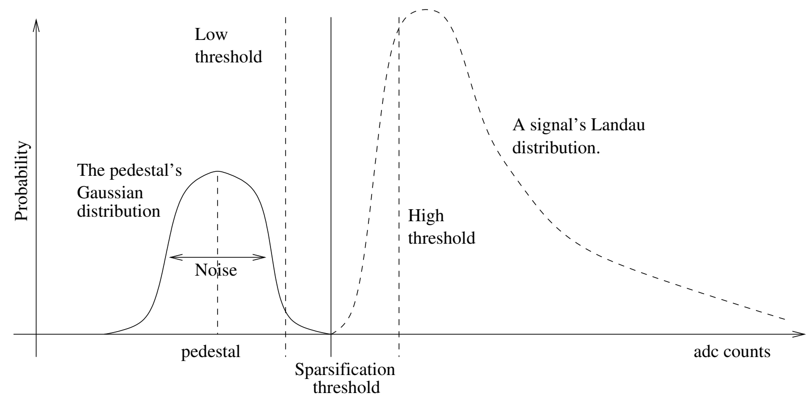

Figure 3.1: *Schematic diagram of pedestal and signal distributions and sparsification threshold.*

It was originally designed for automated testing of svx2 and svx3 die in wafer form but has since been largely used for operating svx2 and svx3 chips on testboards or mounted on hybrids and ladders.

The setup takes advantage of the absence of analog outputs of the tested chips which allows them to be fully controlled and read out without sophisticated analog to digital converting interfaces. In the present system a ***master computer*** generates the patterns via an output register and acquires the data via an input register.

Timing problems between master computer and chip have been solved by adding a custom built interface.

3.2.2 Software

As much as possible of the system has been built out of software. All intelligence is centralized in the master computer, all other hardware serving only as electrical or mechanical interface between the computer and the chips.

The software consists of a set of object libraries. The user must write a specific master program for each new task. It will consist of of a sequence of calls to an appropriate subset of the system routines. All code is written in C.

3.3 Generating signals

In order to make gain measurements or estimations of the signal to noise ratio, a signal has to be provided. Signals were generated by two means.

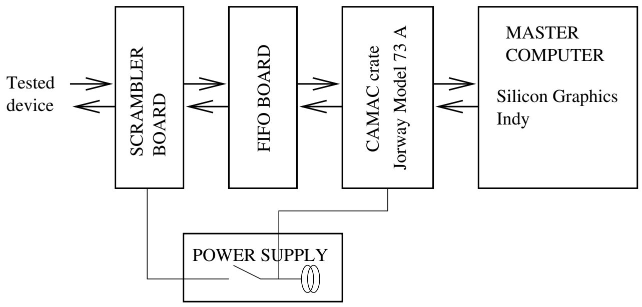

Figure 3.2: ***Schematic overview of the chip testing setup. Pattern files controlling the functioning modes of the readout chips are downloaded from the master computer to a FIFO board and a scrambler. The signals are clocked out to the tested device and the power suppliy. Data returns the same way and is accessible as a file in gray code on the master computer.***

3.3.1 Direct charge injection

The chips are designed so that charge can be injected from a common source into any desired channels. Charge injected channels are selected during initialisation by setting the corresponding calibration mask bit to high. Charge is injected directly to the Preamplifier.

3.3.2 Laser pulses

For testing chips mounted on hybrid and sensor, signals were also generated through laser pulses. A custom built laser diode was mounted on a mobile platform. Lenses were used to focus the laser beam onto the sensor so that only one strip would be hit at focal distance. Neighbouring strips were however affected, yielding signals one tenth in amplitude of the signal directly hit.

As seen in figure 3.3,'the wavelwngth of the laser pulses should be around $1050nm$ to traverse a $300\mu m$ silicon sensor [1]. However lasers in the $1050nm$ region of the spectrum are expensive. A much cheaper $850nm$ laser diode was used, giving a penetration depth of of around $20\mu m$, which is sufficient for testing electronics on one side of a ladder.

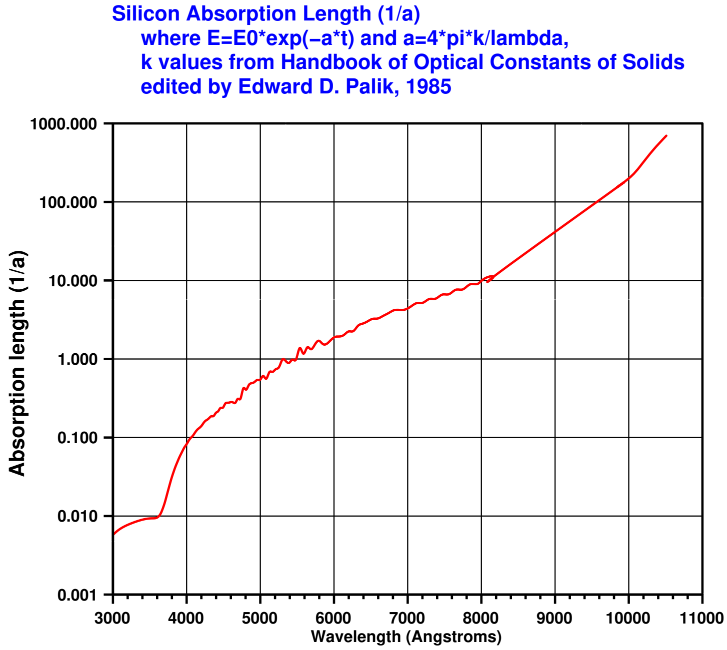

Figure 3.3: *Absorption of visible light in silicon.*

[1]When depleted the sensor will have approximately the same aborbation lengths as bulk silicon.

Chapter 4

Measurements and results

4.1 General outline of the measurements

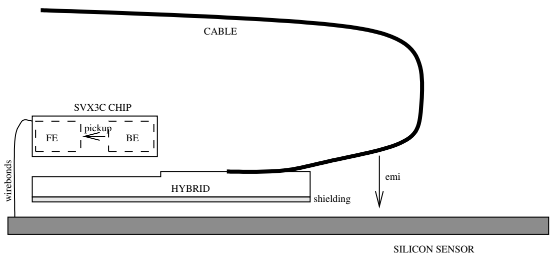

Figure 4.1: *Schematic of a readout chip on hybrid and sensor with cable. The chips wich are connected to the sensor and mounted on a hybrid described in section XXX, are read out, powered and controlled via the cable connected to pads on the hybrid. The cable will be bent over the chips as shown.*

Pedestal shifts with respect to time and to channel number have their origins both inside and outside the readout chips.

Internally, analog pickup and fluctuations in the supplied power can cause variations in the output of the Preamplifier that do not correspond to any input charge. As an example, the Preamplifiers being referenced to ground would treat local fluctuations in the ground plane as charge injection.

Externally, electromagnetic induction can potentially supply charge to the input of the Preamplifiers. This can happen because potential differences are induced between capacitively coupled metal strips on the sensor or because the electromagnetic induction affects the bias voltage which, again, couples capacitively through the MOS-junctions. The former would generate local pedestal shifts while the latter would affect all channels equally.

In order to isolate the different mecanisms at play, separate measurements were conducted for chips mounted on

1. ***test boards***, allowing a closer study of coupling between Front End and Back End within the readout chip,
2. ***hybrid***, making it possible to study effects due to cross-talk between control signals and/or power in hybrid and cable,
3. ***hybrid and sensor***, focusing essentially on the effects of electromagnetic induction on the silicon sensor.

A setup with a chip and a sensor mounted on a test board was also used for studying electromagnetic pickup qualitatively without effects due to cross-talk in hybrid and cable.

4.2 Study of pedestal shifts and noise

4.2.1 Mapping buckets

The principal software tool used in the measurements described below was a program written in C (ref to previous section) henceforth referred to as the ***map*** program. Its purpose is to monitor pedestal variations for charge collected while the Back End goes through a sequence of functioning modes. The possible functioning modes of the Back End are:

1. ***idle mode***: as suggested by the name, the Back End is idle.
2. ***digitization mode***: the digitizing circuitry of the Back End is activated
3. ***readout mode***: data is clocked out by the Back End to the data buses.

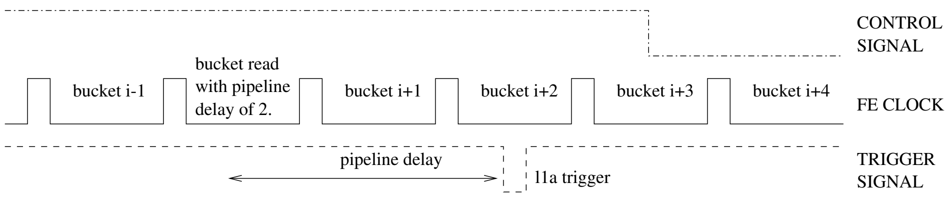

Figure 4.2: ***Front End Clock, l1a trigger and a switching control signal. High clock equals*** $40ns$ ***and low*** $120ns$***. Here the l1a trigger is given in bucket*** $i+2$***. The bucket selected for readout is hence bucket*** i***. The switching of the logic for the control signal occurs in bucket*** $i+3$ ***and cannot affect the data in bucket*** i***.***

As mentioned in (chapter setup), the pattern files used to control the chips contains a digital signal called the Front End clock (fig. 4.2) which controls the pipeline. In the actual experiment it will be synchronized with the beamcrossings. Switching the logic state of the Front End clock (immediately after a beam crossing) will cause any incoming signal to be stored as charge on a new cell of the pipeline (ref to chip description). The 46 cells of the pipeline are used in a continuous loop. The map program ignores the periodic looping of the pipeline and considers the output as a continuous sequence of ***buckets***.

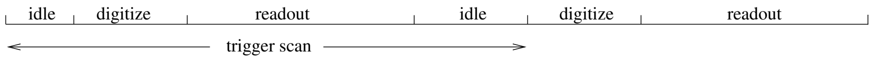

Figure 4.3: ***The idle-digitize-readout mode sequences imposed to the Back End of the readout chip by the map program and l1a trigger scan of the first sequence.***

The map program builds a pattern containing two idle-digitize-readout control sequences. The level 1 accept (l1a) trigger tells the readout chip to digitize and readout the signal stored in one of the buckets of the pipeline. Which is determined by the pipeline delay. In figure 4.2, the pipeline delay is 2 and a l1a trigger in bucket $i + 2$ will cause the information stored in bucket i to be digitized. The l1a trigger is filled in the pattern by a loop in the program allowing it to scan through the first idle-digitize-readout (HOW MANY ELECTR) sequence as indicated in figure 4.3. The second sequence is used to digitize and retrieve the data resulting from the scan of the first.

The map program gives an idea of how chip operation might affect data acquisition. It does not however provide a foolproof simulation of how the detector will function in the RunII environment.

4.2.2 Chip on testboard: study of coupling between Front End and Back End

In this first series of studies the chip was mounted on a custom made test board and tested with the setup described in the previous chapter (ref to Patt02 board) using the map program described above.

Figure 4.4 shows the output of a Svx3 readout chip when the Back End is idle, in digitize mode and in readout mode.

The pedestal is fairly constant when the Back End is idle. Shifts in pedestal are smaller than 4 ADC counts. When the chip enters digitize mode, the amplitude of the shifts increases and is at its worst when passing from digitize mode to readout mode. The maximum amplitude of the Pedestal shifts is 18 ADC counts. No charge is being injected.

The variations are due to fast switching of digital signals in the Back End coupling to all Preamplifiers of the Front End. This coupling could occur via the groung plane or the power supplies. No systematic attempts were made to reduce coupling on the testboard.

All channels are affected equally by the coupling to the Back End signals as suggested by figure 4.5 where the pedestal versus channel number is represented for the 50 first buckets filled during readout mode. The pedestal shifts are common to all channels except for three which are malfunctioning.

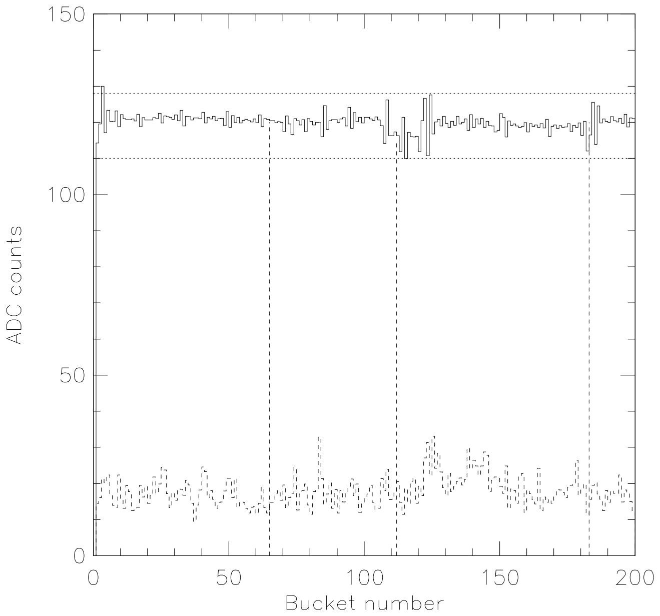

Figure 4.4: *Average pedestal (solid) and RMS noise (dashed) versus cell number for a chip on testboard. Noise is multiplied by a factor 20. The Back End is idle until bucket 65 where it enters digitization mode. Readout starts in bucket 112 and ends in bucket 183. Noise remains around one count throughout the sequence while the pedestal varies by 5 ADC counts or less until the end of readout. Variations are more important at the beginning of readout where they reach 18 ADC counts in amplitude. The preamplifier bandwidth was set to 7.*

4.2.3 Chip on hybrid: study of cross-talk in hybrid and cable

Figures 4.6 and 4.7 show the same as figures 4.6 and 4.7 respectively but for a readout chip mounted on a Svx3 hybrid (layer 1).

Far from revealing any effects of coupling between signals in the cable or in the hybrid, mapping of the chip on hybrid (4.6) shows even smaller variations of the pedestal versus bucket number than for the chip on testboard.

Figure 4.7 shows a sagging of the pedestal towards the left, i.e. for the first of the 128 channels read out by the chip.

4.2.4 Chip on hybrid and sensor: study of electromagnetic induction and sensor defects

Electromagnetic induction

When the readout chips were mounted on hybrid and sensor, mapping of the buckets with the map program revealed much larger fluctuations in pedestal versus bucket number than ever seen with the chip on test board or on hybrid (see fig 4.8). The variations were most important during readout where RMS noise went up to 8 ADC counts, that is to say 5600 EC.

Unlike the variations observed for the chip on testboard and the chip on hybrid, the pedestal shifts obseved with the chip mounted on hybrid and sensor displayed big differences from one channel to another. Figure 4.8 shows the variations in pedestal versus bucket number for channels 140 and 200, that is to

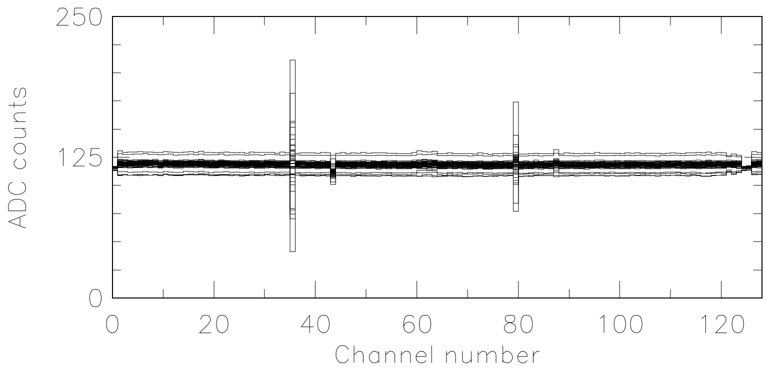

Figure 4.5: ***Envelope for the chip on testboard: the pedestal versus channel number has been plotted for the 50 first buckets of the readout sequence. A part from a few defectuous channels, the variation are the same for all channels and the variations from one bucket to another do not exceed 25 ADC counts in amplitude. The preamplifier bandwidth was set to 7.***

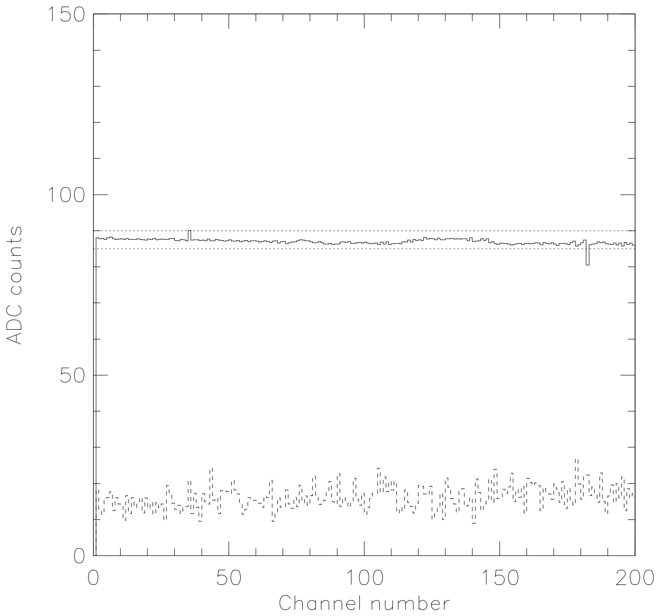

Figure 4.6: *Average pedestal (solid) and RMS noise (dashed) versus cell number for a chip on testboard. Noise is multiplied by a factor 20. The Back End is idle until bucket 65 where it enters digitization mode. Readout starts in bucket 112 and ends in bucket 183. Noise remains around one count throughout the sequence while the pedestal varies by 5 ADC counts or less until the end of readout. Variations are more important at the beginning of readout where they reach 18 ADC counts in amplitude. The preamplifier bandwidth was set to 7.*

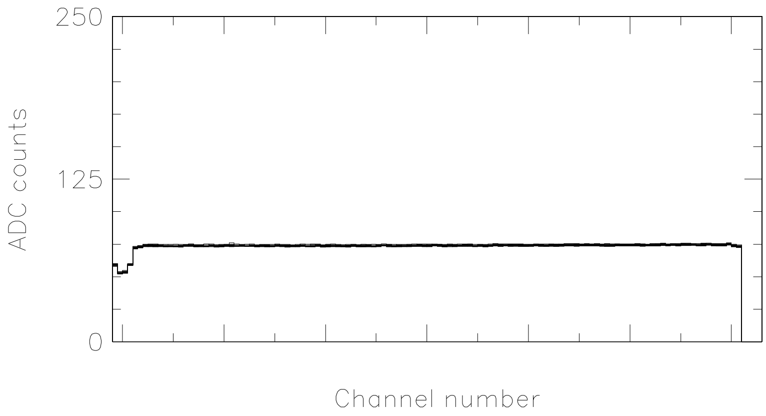

Figure 4.7: ***Envelope for the chip on testboard: the pedestal versus channel number has been plotted for the 50 first buckets of the readout sequence. A part from a few defectuous channels, the variation are the same for all channels and the variations from one bucket to another do not exceed 25 ADC counts in amplitude. The preamplifier bandwidth was set to 7.***

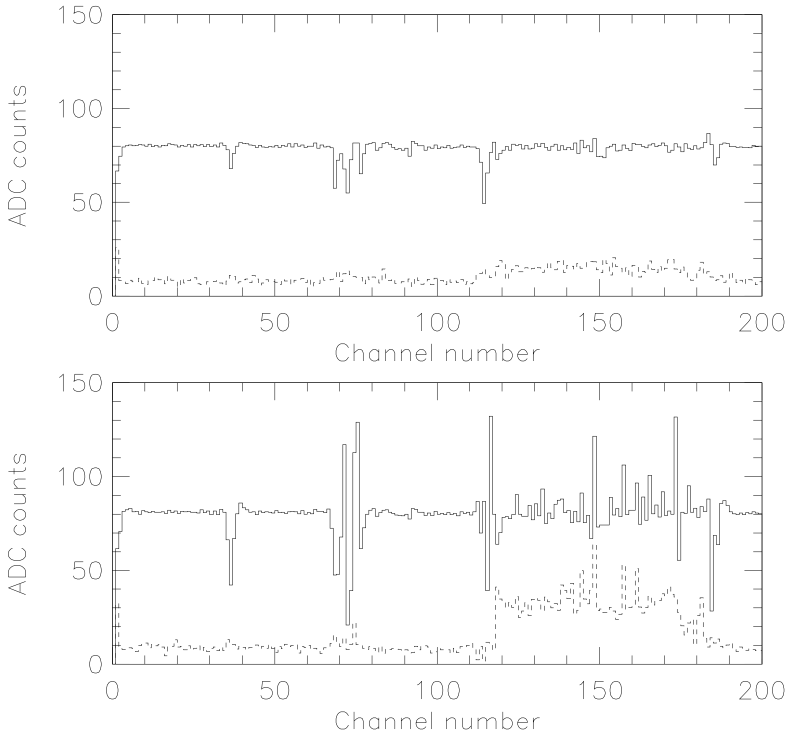

Figure 4.8: *Average pedestal (solid) and RMS noise (dashed) versus bucket number for two channels of the second ϕ-side chip of a layer 0 ladder. The chip is mounted on a Svx3 hybrid and connected to one sensor. The upper plot is that of channel 140 near the edge and the lower that of channel 200 in the middle. Noise is multiplied by a factor 5. The Back End is idle until bucket 65 where it enters digitization mode. Readout starts in bucket 112 and ends in bucket 183. The preamplifier bandwidth was set to 2 and the bias voltage applied to the sensor was* $40V$.

say channels connected respectively to a strip near the edge and a strip near the middle of the 128 strips read out by the second ϕ-side chip of a layer 0 ladder.

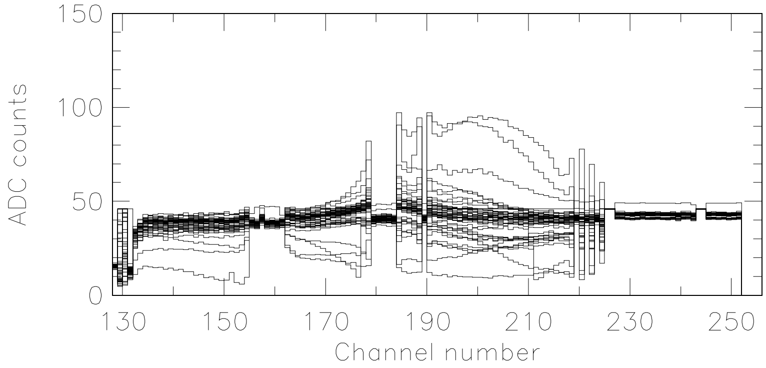

Figure 4.9: ***Pedestal versus channel number for the 50 first buckets of the readout sequence for the second of two readout chips mounted on a layer 0 hybrid on the ϕ-side of a layer 0 sensor. Channels 179 to 183 and channel 189 are not connected to the sensor. Channels from 218 and upwards are only partially bonded and should be negelected. Channels 154 to 162 are believed to be affected by broken MOS-junctions in the sensor. Clearly time-varying structures can be observed towards the middle of of the 128 channels. The preamplifier bandwidth was set to 2 and the bias voltage applied to the sensor was*** $40V$.

Plots of pedestal versus channel number for different buckets clearly shows time varying structures. Figure 4.9 shows the structures in pedestal versus channel number for the fifty first events during readout for the second ϕ-side chip of a layer 0 ladder. The structures and the variations in structure are at their peak during the beginning of readout. Figure 4.9 therefore gives an idea of the envelope of the variations and should be compared to figure 4.5 showing the same plots obtained for a chip mounted on a testboard.

Unbonded channels in figure 4.9, such as channels 179 to 183 and channel 189, are not subject to the same variations with bucket number as their neighbouring bonded channels. This would indicate that the time-varying structure of the pedestal versus channel number would be caused by the sensor.

The sensor can theoretically generate unwanted pedestal shifts in three different ways:

- defects in the silicon, such as the punch-through effect described below, would affect the structure of pedestal and RMS noise versus channel number. The effect should however be more or less time independent.
- power and ground could pick up signals or simply be noisy. Time dependent variations would be transmitted to the readout chips where they should affect all channels equally.

- external electromagnetic pulses could induce charge onto the strips of the sensor. These electronic pulses would be treated as normal input to the preamplifier. Differences in amplitude of the electromagnetic pulse at different strips would generate pedestal shifts of unequal amplitude at the corresponding readout channels.

The dependence in channel number of the time-varying structure clearly favours last explanation. The geometry of the of the structure also hints that the source of the electromagnetic pulses is the cable.

The cable is split in two, each part carrying different control signals. For the tested ϕ-side of the layer 0 ladder [1], each part of the cable passes over the middle of the 128 strips read out by each chip.

Additional support for this explanation is provided by the effects of shielding described below and close monitoring of the effects of various signals passing in the cable by lifting them out to otherwise idle parts of the pattern.

In figure 4.10 we have plotted the pedestal versus channel for a bucket where we know that a signal using the bus0 channel of the cable switches logic state. Data points are represented as black squares with error bars. As for previous plots channels 179 to 183 and channel 189 are different since they are not bonded to the sensor. The unbonded channels also affect neighbouring channels. The structure is however clear for remaining channels. The dotted curb is a gaussian fit and should be seen a a first approximation.

We obtain the same structure (fig. 4.10) if we study a bucket where a similar signal, using the neighbouring bus1 channel of the cable, switches logic state. Pedestal versus channel number is represented as white squares on the same figure.

Figure **??** shows a simplified MATLAB modelisation of the measurements represented in figure 4.10. The model used is that of a simple wire over the sensor. The charge induced onto the sensor strips is taken to be proportional to the strength of the electromagnetic pulse when it reaches them. The pulse decreases with the radial distance to the wire as $\frac{1}{r^2}$. The presence of the unbonded channels and their effect on neighbouring channels has been taken into consideration.

This very simplified model, focusing solely on the effects of electromagnetic induction from the cable, shows a good agreement with data.

If the switching in logic state of the two signals described previously occurs in the same bucket the total variation in pedestal will be the sum of their respective contributions shown in figure 4.10. For each bucket, the contribution of electromagnetic induction to the structure of the pedestal versus channel number will be a linear combination of the contributions from all signals travelling through the cable.

To evaluate the contribution of each signal, a special setup was arranged where a sensor was directly connected to a readout chip, thus allowing a better

[1] The ladder tested here is not complete as it only consists of one sensor and since readout electronics and cable are only mounted on one side of this sensor.

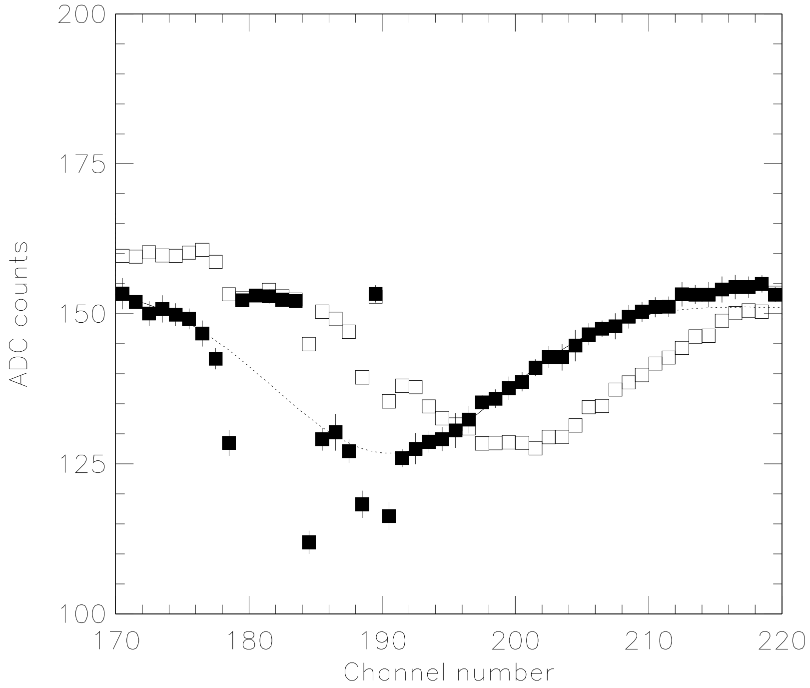

Figure 4.10: ***Pedestal versus channel number for two buckets where known signals are switching logic state. The two signals, active at the end of the digitization sequence, are using respectively the bus0 and the bus1 channels of the cable. The preamplifier bandwidth was set to 2 and the bias voltage applied to the sensor was*** $40V$.

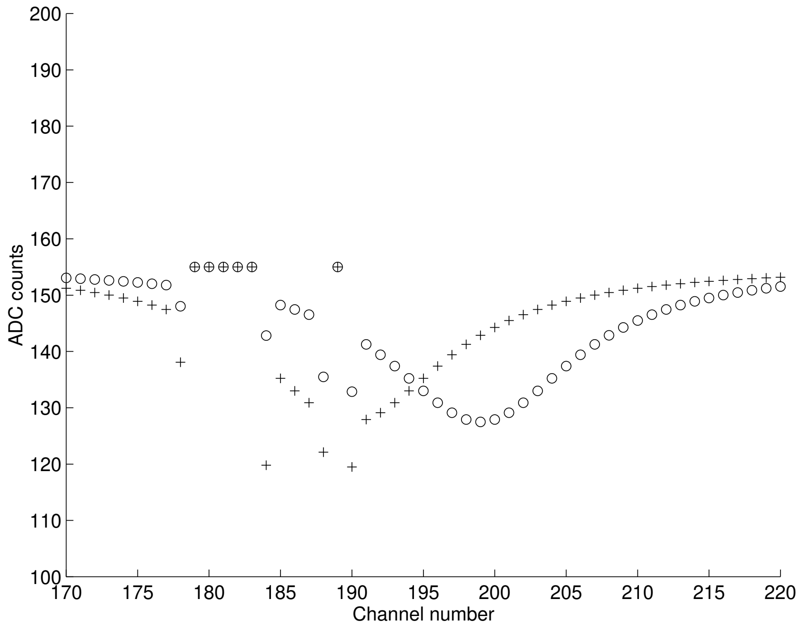

Figure 4.11: *simplified MATLAB modelisation of the measurements represented in figure 4.10: pedestal versus channel number as a result of electromagnetic induction. The model used is that of a simple wire over the sensor. Non bonded channels and their effect on neighbouring channels have been taken into consideration.*

control over ground and power and excluding any effects caused by the presence of the hybrid. An insulated copper wire was aligned on the sensor strips stretched one centimeter over the surface of the sensor. The map program was then run with this cable attached to each control channel in turn. The maximum amplitude of the variation in pedestal is entered in the table of figure 4.12 for each control signal.

The main culprits appear to be the $5V$ AC signals since they generate the largest pedestal shifts. However they occur only a couple of times during each sequence. The $3V$ AC signals cause smaller pedestal shifts but occur more often. They are also more likely to occur together in a same bucket yielding a much higher total pedestal shift.

The increase in RMS noise during readout is most important for channels affected by the cable carrying the data buses (fig. 4.8). This is due to the random nature of the data transfer. The data bits, implying switches in logic state and pedestal shifts similar to those of the control signal in figure 4.10, come randomly.

Reducing the effects of electromagnetic induction

To reduce the amplitude of variations in pedestal that can be linked to electromagnetic induction from cable to sensor, one has to reduce the amplitude of electromagnetic pulses reaching the sensor. This can be achieved by either

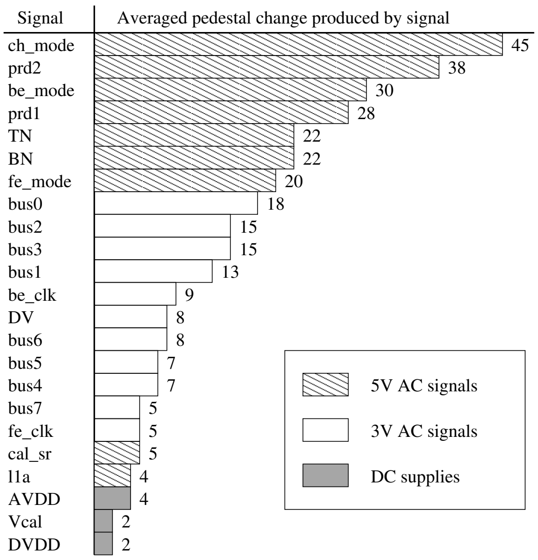

Figure 4.12: ***Electromagnetically induced signals by different signals travelling in the cable. The test was done by running the map program with a naked copper wire copper wire connected to one signal at a time.***

reducing the amplitude of the electronic signals in the cable or damping the resulting electromagnetic pulses through shielding.

Smaller AC signals are allready planned for the real run.

Elementary attempts at shielding were made by folding a thin aluminum foil around the cable. In figure 4.13, the pedestal has been plotted versus channel number for 30 buckets in the readout sequence, starting 10 buckets after the beginning of readout. Time varying structures are eclusively due to linear combinations of $3V$ data bits passing in the data buses of the cable. Mamimum variations have been reduced from 75 ADC counts to 55 ADC counts, giving an attenuation of 26%.

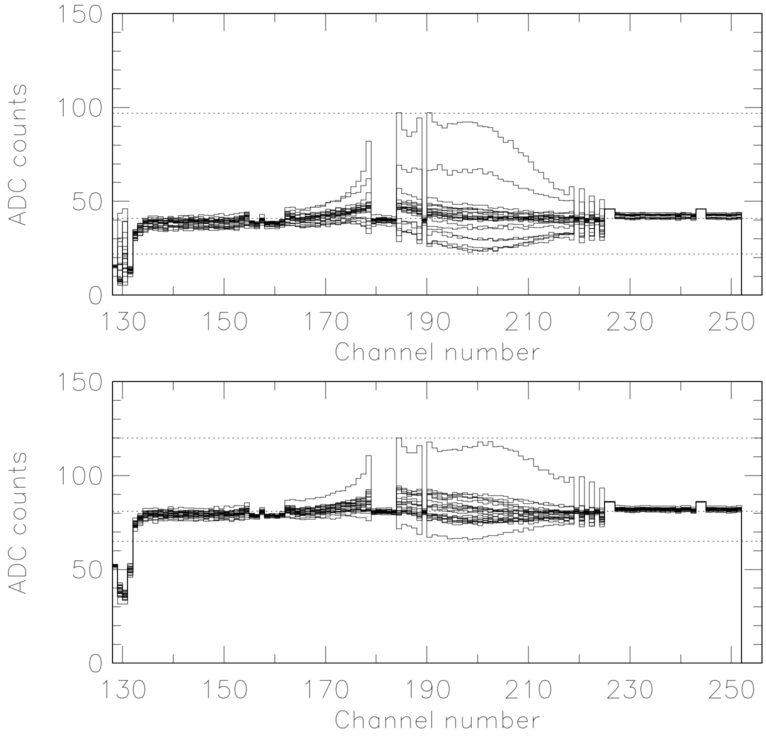

Figure 4.13: ***Before and after elementary shielding. Both figures show the pedestal versus channel number for the second of two readout chips mounted on a layer 0 hybrid and the ϕ-side of a layer 0 sensor. For the upper figure the cable is naked and for the lower a thin aluminum foil has been folded around the cable and connected to the hybrid ground. Channels 179 to 183 and channel 189 are not connected to the sensor. Channels from 218 and upwards are only partially bonded and should be negelected. Channels 154 to 162 are believed to be affected by defects in the sensor. The preamplifier bandwidth was set to 2 and the bias voltage over the sensor was*** $40V$.

Defects in the sensor: punch-through effect

4.3 Laser study results

The laser diode setup described in (ref to previous section) was used to test whether real signals were affected by dead-timeless operation beyond simple pedestal shifts. For example the gain could be influenced by coupling. Using the level 1 accept as a trigger for the laser diode, a laser pulse injected charge into a specific channel for every bucket scanned by the map program.

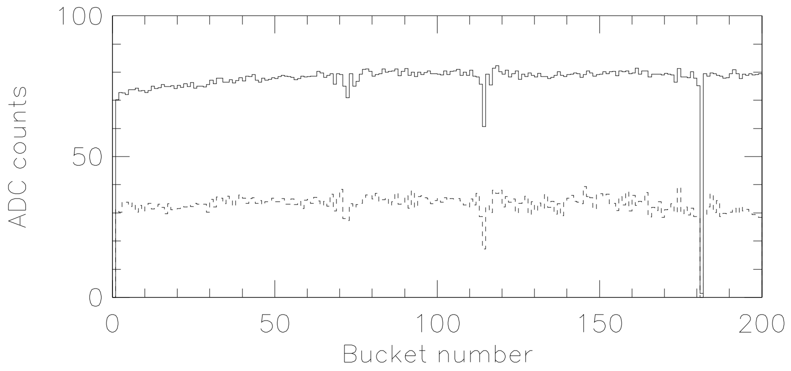

Figure 4.14: ***Difference between the output of the channel directly hit by the laser pulse and a channel not affected by the pulse for two pulse intensities. The variations around the beginning of digitization (bucket 67) and the beginning of readout (bucket 112) is of the constant amplitude and is believed to be direct pickup by of the current pulse feeding the laser diode. Apart from these variations and a "dead bucket" due to a control signal at the end of readout (bucket 183), the remaining variations are less than*** 10% ***and could be due to fluctuations in the laser output.***

Figure 4.14 shows the difference between the output of the channel directly hit by the laser pulse and a channel not affected by the pulse for two pulse intensities. The variations around the beginning of digitization (bucket 67) and the beginning of readout (bucket 112) is of the constant amplitude and is believed to be direct pickup by of the current pulse feeding the laser diode. Apart from these variations and a "dead bucket" due to a control signal at the end of readout (bucket 183), the remaining variations are less than 10% and could be due to fluctuations in the laser output.

Appendix A

Semiconductors and junctions

A.1 Semiconductors

In chemical terms a semiconductor crystal is a giant covalent molecule. No single atom has a significant effect on the electron energies. The latter are contained within two energy bands, the valence band and the conducting band, separated by a forbidden energy region, the energy gap (fig.A.1). The valence band corresponds to bonding electron orbitals and the conducting band to antibonding orbitals.

For silicon, the gap energy ΔE is $1.1eV$.

At low temperatures and in the absence of impurities, i.e. for an ***intrinsic*** semiconductor, the valence band is full and the conducting band is empty. If an electron absorbs the energy $E > \Delta E$, it can enter the conducting band leaving a ***hole***, or positive charge, in the valence band.

Electron and hole distributions are governed by Fermi-Dirac statistics, letting the probability of an electron having the energy E vary as:

$$f(E) = \left(1 + e^{E-E_F/kT}\right)^{-1} \tag{A.1}$$

Where E_F is the Fermi energy defined as $f(E_F) = \frac{1}{2}$.

A.2 Doped semiconductors

The properties of a semiconductor can be altered by the addition of impurities, i.e. ***doping***. Doping is explained beneath for the case of silicon.

Silicon is a type IV material with four valence electrons. If an atom of a type V material is inserted in the silicon lattice, only four of its five valence electrons will be used for covalence bonding with the neighbours. The fifth electron will act as an extra charge carrier [1]. Hence, an impurity of a type V material is referred to as a *donor*.

Doping with a type III material (three valence electrons) will, conversely, leave a hole in excess, and the added impurity is called an *acceptor*.

If electrons are majority carriers, the silicon will be said to be *n-type* and, if holes are majority carriers, it will be *p-type*.

We define n as the number of electron carriers and p as the number of hole carriers.

For intrinsic semiconductors:

$$n = p = n_i$$

For doped semiconductors:

$$n \neq p$$

A typical doping level for lightly doped $n-$ and $p-type$ materials is around $10^{16} cm^{-1}$. When the doping exceeds $10^{16} cm^{-1}$ one speaks of heavy doping and the material is referred to as p^+- or n^+-type.

The typical concentration of atoms in silicon is $5 \times 10^{22} cm^{-1}$.

Impurities create additional energy states within the forbidden band and induce shifts of the Fermi energy E_F (fig. A.2). For $n-doped$ materials:

[1] A charge carrier is an electron or hole in the conduction band.

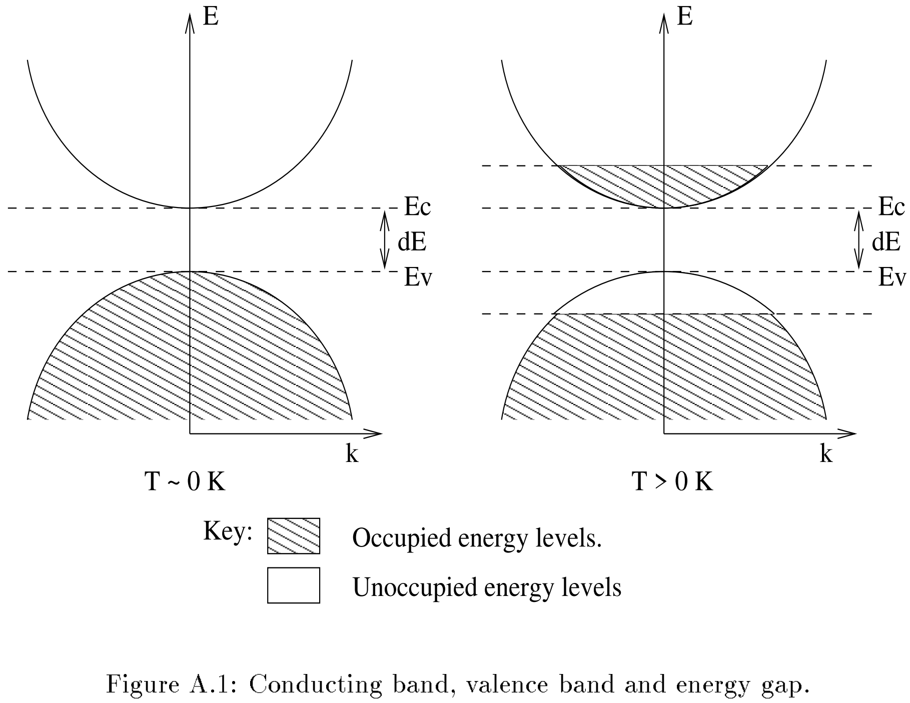

Figure A.1: Conducting band, valence band and energy gap.

$$E_F = E_i + kTln(\frac{N_D}{n_i})$$

For $p - doped$ materials:

$$E_F = E_i - kTln(\frac{N_A}{n_i})$$

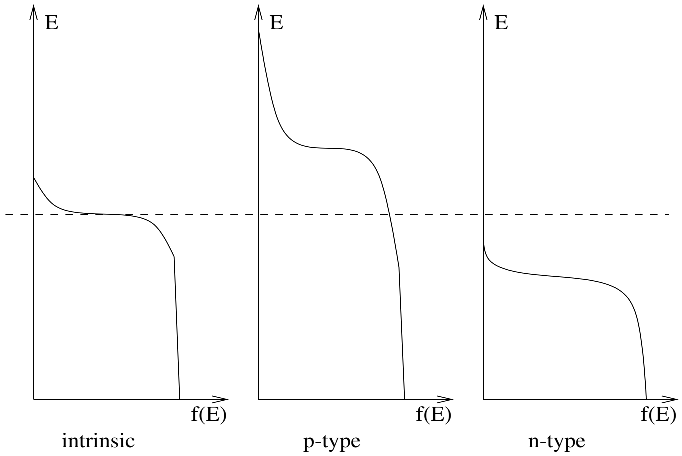

Figure A.2: Shifting of Fermilevels as a result of doping.

A.3 $p^+n - junctions$

When a $p - type$ material and a an $n - type$ material are brought into contact, two competing currents will result at the interface, also known as the *junction.* Electrons from the $n - type$ material diffuse into the $p - type$ material where they are neutralized by the holes. They leave behind inonized impurity atoms on both sides of the junction. [2] These fixed charged atoms give rise to an electric field that acts as a barrier that tends to keep holes on the p^+-side and electrons on the n-side. The net outcome is a thin *depletion region* at the junction. The depletion region has no charge carriers and can thus have an electric field $\vec{E}$.

The $pn - junction$ has a diode characteristic (fig. A.3). When a voltage is supplied with the negative pole on the n-side and the positive on the p-side, a steady current will flow. This happens because movable carriers are pushed towards the interface where they recombine. This is called the *forward biased condition.*

If the polarity is inverted, electrons and holes are pulled apart thus increasing the depleted region. This is referred to as the *reverse biased condition.* Only

[2]The diffusion of holes from the $p - type$ material to the $n - type$ material has the same effect.

a small reverse bias current is flowing. This current becomes a limiting factor when the *pn*-junction is used in a detector [3].

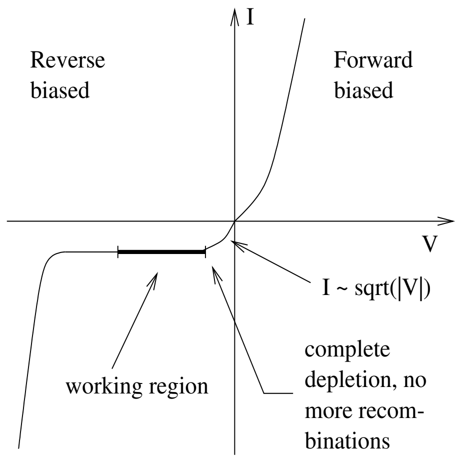

Figure A.3: A basic semiconductor detector is a reverse biased diode.

A.4 MOS-junctions

Metal Oxide Silicon junctions also play an important role in the SVXII silicon sensors. A simplified image of a MOS-junction is that of a homogeneous *p*-type semiconductor insulated from metal by an insulator, SiO_2.

As used in the SVXII sensors, the MOS-junctions function as capacitances between p^+-implants and metal strips [4], cutting off DC-currents.

[3] It is due to thermal generation of charge carriers in the space charge region and diffusion of minority carriers from the neutral regions into the depleted region.

[4] The metal strips are connected to the readout chips described below.

Appendix B

Particles passing through matter

Moderately relativistic particles lose energy in matter primarily by ionization. If the incident particle velocity βc is larger than that of orbital electrons ($\sim Z\alpha c$). and small enough that radiative effects do not dominate, then the mean rate of energy loss is given by the *Bethe-Bloch* equation,

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left(\frac{1}{2}ln\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2} - \beta^2 - \frac{\delta}{2}\right) \tag{B.1}$$

Bibliography

[1] The CDF II collaboration (1996).
The CDF II Detector, Technical Design Report.
FERMILAB–Pub–96/390–E

[2] Max J. O. Strutt (1966).
Semiconductor devices.

[3] B.R. Martin and G. Shaw (1992).
Particle Physics.
John Wiley and Sons

[4] Alan M. Litke and Andreas S. Schwarz (1995).
The Silicon Microstrip Detector.
Scientific American, May 1995

[5] F. Abe et al. (1995).
Observation of Top Quark production in $p\bar{p}$ collisions with the collider detector at Fermilab.
Physical Review Letters, Vol. 74, No 14, pages 2626-2631, April 3 1995

[6] Tony M. Liss and Paul L. Tipton (1995).
The Discovery of the Top Quark.
Scientific American, September 1997

[7] M. Garcia–Sciveres, D. Ray (1998).
Documentation for the PATT board.
LBNL, unpublished.

[8] M. Garcia–Sciveres.
Readout electronics architecture and packaging for the CDF silicon upgrade.
Nuclear Instruments and Methods in Physics Research, A 392 (1997) 375-379