CDF/DOC/SEC_VTX/PUBLIC/4852

Statistical Study of SVX3D Chip Dynamic Pedestal Subtraction Threshold Level

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Jan 14 1999

1 Objectives – definitions

1.1 Dynamic pedestal subtraction

The SVX3D chip has a modified Wilkinson type analog to digital converter (ADC). Its analog part is a shared voltage ramp connected to a comparator for each channel. The digital part is a counter that does not necessarily have to be started simultaneously as the ramp. The comparator output for a channel will go high when the ramp voltage reaches the measured signal level of that channel. At that time the corresponding digital counter's value is latched into a memory cell. The design is shown in figure 1.

The ADC is capable of performing a common mode (pedestal) subtraction in real time known as Dynamic Pedestal Subtraction (DPS). This is done by starting the digital counter when a certain number of comparators have gone high. This number is referred to as the DPS threshold. If sufficiently many channels do not carry signal, i.e. are at pedestal, the counter will be started somewhere near the pedestal level, setting the zero point of the digital scale at that level. The effect is that the pedestal level will be subtracted from the measured signal.

The motivation for subtracting the pedestal level is that many contributions to noise, for example electromagnetic pickup, can influence all channels on a chip collectively, as common mode noise. In CDF, the only way to subtract that kind of noise is to do it on the chip, since pedestal information is lost when data is read out in sparse mode.

The sparsification works by reading out only channels carrying digital signal above a sparsification threshold and, optionally, their neighbors (neighbor logic). The purpose of sparsification is to keep readout time down. Sparsifica-

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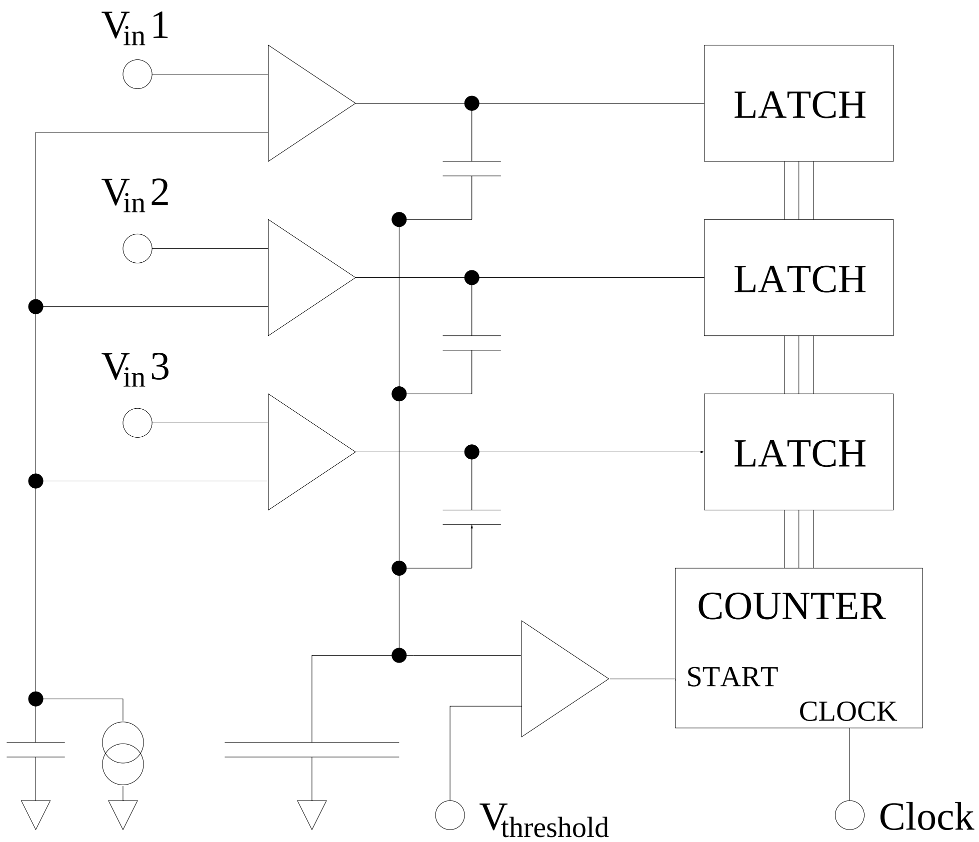

Figure 1: Wilkinson ADC with DPS circuitry.

tion and DPS have to be considered together as it is their combined effect on chip performance that has to be optimized.

1.2 Gain

The conversion of charge into digital numbers is described by an overall gain. The gain used here is $\frac{1}{545} ADC\, counts/e^-$. With a smaller gain (more electrons per count) resolution deteriorates. It is relevant for the discussion here that the gain is large enough that the pedestal distribution is spread out over several ADC counts. If that were not the case chip noise would be dominated by the binning coarseness.

1.3 Statistical noise

Dynamic pedestal subtraction adds noise to the digitized signal. The origin is statistical fluctuations in the zero level set by the DPS. The signal measured with DPS turned on is the difference between actual signal and the reference point set by the counter start. Fluctuations in pedestal channels shift the starting point of the ADC counter somewhat and the unwanted shifts in starting point translate directly into noise in the digital signal.

The charge in channel i (C_i) is presented to the ADC by the analog part of the SVX3D chip as a voltage (V_i). Through the voltage ramp the comparator translates voltage into a point in time (T_i)[1]. The digital counter will start at time t_D, given by[2]

$$t_D = smallest\, t : |\{T_i \leq t\}| \geq D, \tag{1}$$

where D is the DPS threshold expressed in channels. If the T_i are regarded as stochastic variables, then $t_D(T_1, T_2, ...T_{128})$ defines a stochastic function. The RMS statistical noise added by the DPS to the output signal, is just the standard deviation of t_D:

$$noise(D) = Dev(t_D),$$

where time is measured in appropriate units, such as ADC counts.

1.4 Efficiency

Channels carrying signal will be lost, not read out, if they fall below the combined effects of the DPS subtraction and the sparsification threshold, S. There is always a probability that signal is lost this way, but more signal is lost if the counter start t_D is shifted upwards. That is the case when fewer channels than the DPS threshold are at pedestal; the digital counter start will be greatly delayed as the counter will not be started by a pedestal channel, but rather by a signal-carrying or noisy channel. Efficiency is defined as the ratio of the number

[1] Ideally, T_i will be a linear function of C_i.

[2] Here $|\{x\}|$ just means "the number of x", $\{x\}$ being the set of x and $|\cdot|$ the cardinality operator.

of signal channels read out to the total number of signal channels. If neighbor logic is not taken into account the efficiency will simply be given by:

$$\begin{aligned} H &:= \{i \in [1,128] : i\, carries\, signal\} \\ efficiency(D,S) &= \frac{|\{i \in H : (t_i - t_D(t_1, ..., t_{128})) \geq S\}|}{|H|} \end{aligned}$$

1.5 Noise occupancy from sloped pedestal

A sloped pedestal is one where some disturbance superposes a non-constant charge distribution on top of the "real" charge distribution. The simplest case is a linear slope where charge corresponding to $-s$ counts is added to the left end and $+s$ to the right end of a chip. Noise occupancy are the pedestal channels that (due to the combined effects of slope and amplifier noise) are above the sparsification threshold and thus read out. It is desirable to minimize noise occupancy in order not to overload the readout system. Without the neighbor logic, the noise occupancy per chip is:

$$noise\, occupancy(D,S,s) = \left|\left\{i \in \widehat{H} : (t_i - t_D(t_1, ..., t_{128})) \geq S\right\}\right|$$

2 Variables

2.1 Relationships

The number of channels, D, required to start the ADC counter has been considered an independent variable so far. It is in fact determined by the common reference level of the comparator shown in figure 1. That level is in turn set by an external resistor connected to the chip. The relationship between resistance and the resulting external voltage input to the chip has been measured, as well as the relationship between that voltage and the number of channels required for counter start. The internal voltage cannot be directly measured. Together the measurements yield a translation function between resistance and DPS threshold.

2.2 Resistor and external voltage

The external resistor controls a current that is mirrored in a chip internal circuit, through a transistor coupling known as a current mirror. This internal current produces the comparator reference voltage as a voltage drop over an internal resistor. The connection is such that a larger external resistor gives a smaller current and therefore a lower reference voltage for the comparators.

The relationships are in a first approximation

$$D \propto U_{internal} \propto I \propto \frac{1}{R_{external}}.$$

Measurements of the relationship between external voltage and resistance show that an exponential curve fits well. See figure 2. The behavior of an irradiated chip differs from that of an non-irradiated chip in that the external voltage is lower for the irradiated chip, with the same resistor connected.

2.3 Voltage and number of channels

The charge injection feature of the SVX3D chip can be used to give some channels a high signal, while others remain at pedestal. If the counter is started by the pedestal channels the charge injected channels will be clearly visible. If the number of channels with charge injection is increased, at some point there will not be enough pedestal channels left to start the counter, and the readout from the signal channels will drop to zero or almost zero. This way it is possible to determine how many channels are required to start the counter for a certain external voltage. The result is shown in figure 3.

If resistance is translated into voltage using the fitted exponential, figure 3 turns into figure 4. No difference between irradiated and non-irradiated chips was found in the voltage–threshold relationship.

2.4 Checks on predictability

Only one irradiated and one non-irradiated chip were measured with regard to the resistor–voltage function.

Using charge injection in different channels and monitoring the readout it was found that:

1. The required number of channels does not depend on which channels are kept at pedestal. Only the number of channels matter.

2. The required number of channels for a certain voltage is constant. It does not exhibit fluctuations within a five-minute time scale.

3 Statistical computations

3.1 Method

Described here are some simple computations of DPS performance. The probability distribution for the charge input is assumed to be identical and independent for all channels in a chip. From this the distribution of the DPS subtraction point is calculated. From the combined effect of DPS and sparsification threshold the performance parameters efficiency and statistical noise are evaluated.

Using a deterministic model of charge distribution, noise occupancy from pedestal slope is investigated.

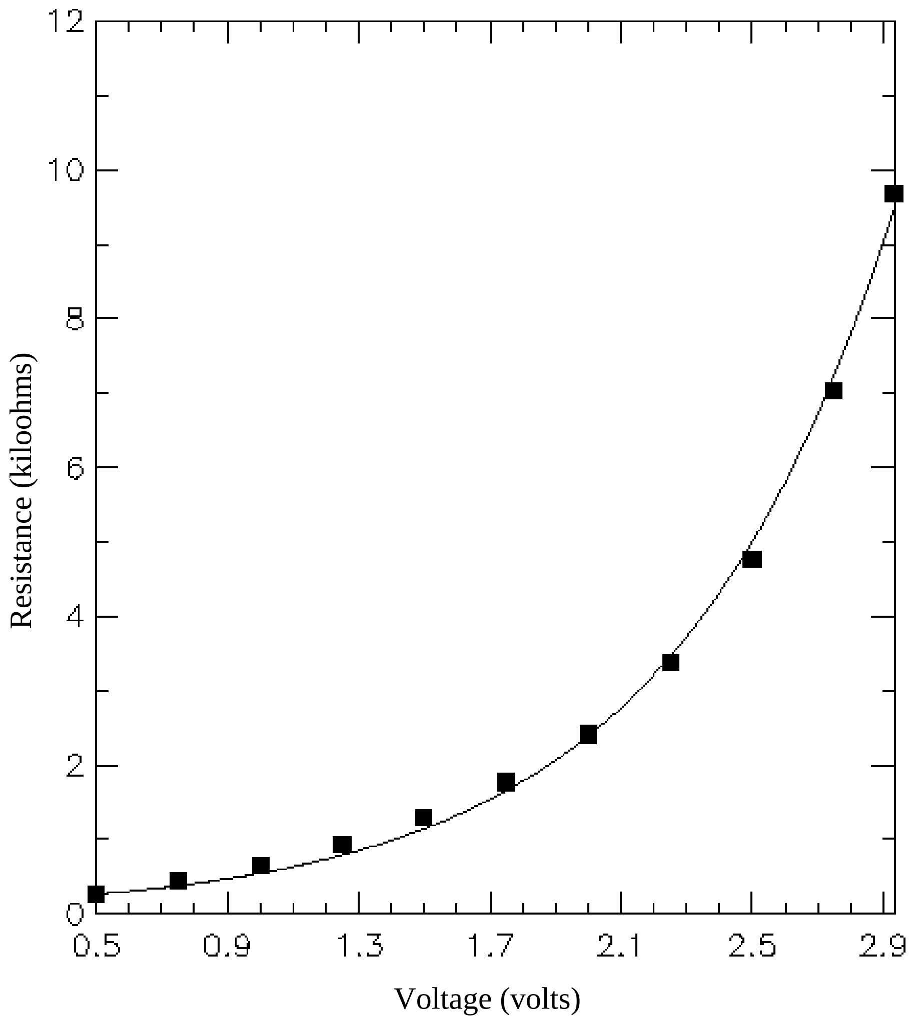

Figure 2: Functional relationship between resistance and voltage. Here resistance is plotted as a function of voltage for an irradiated chip. Also shown is a fitted exponential curve.

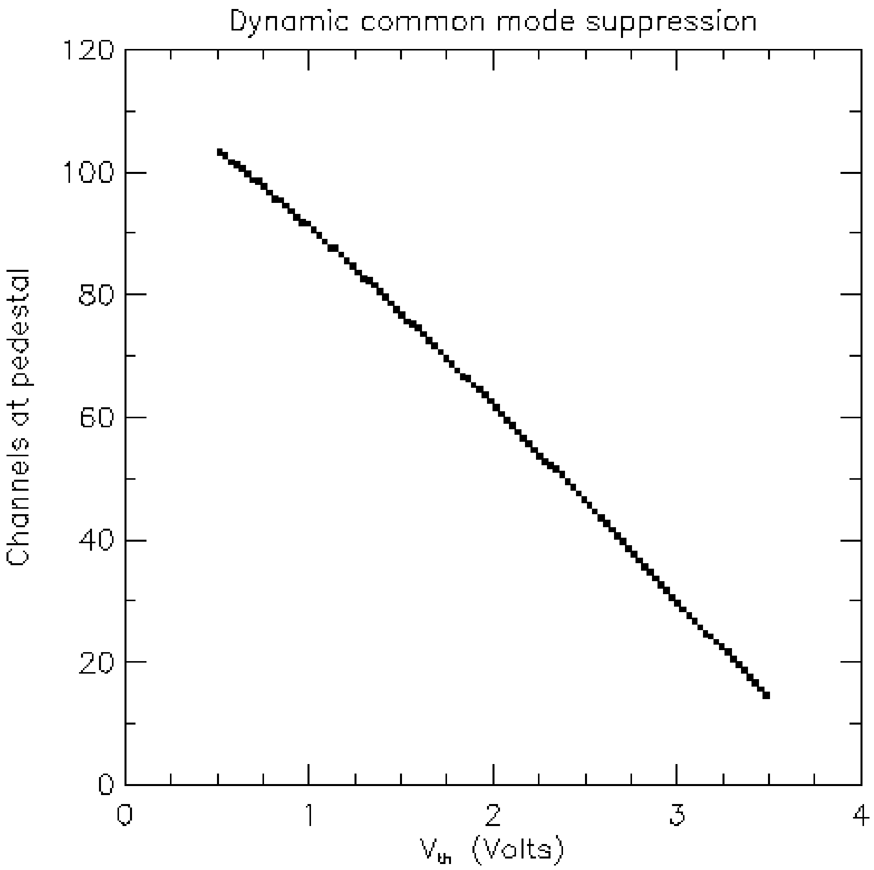

Figure 3: Channels required to start counter as a function of input voltage.

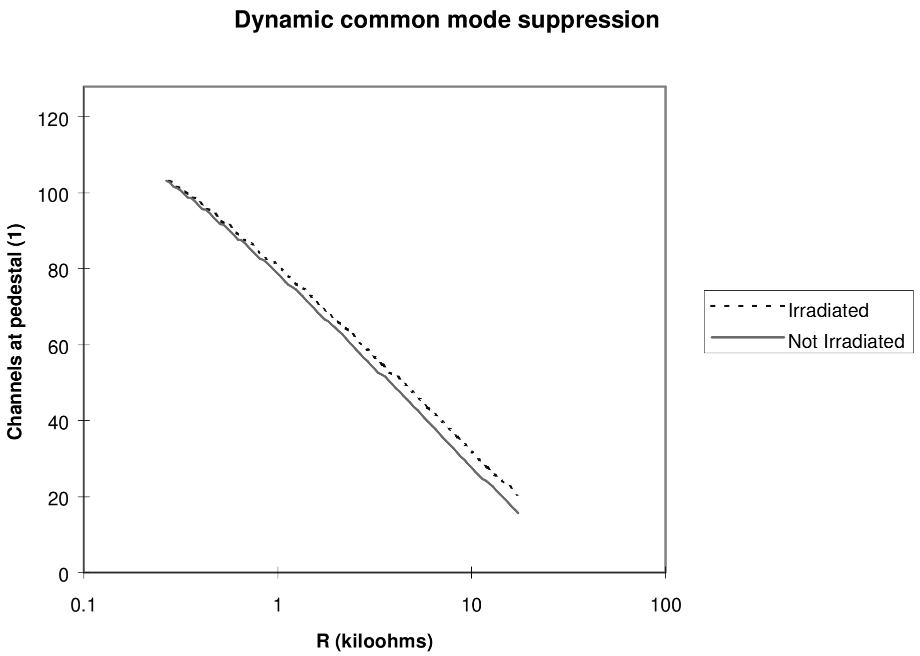

Figure 4: Number of channels required to start counter as a function of the external resistor. Both the non-irradiated an irradiated case is shown. The dose of the irradiated chip was 3.8 $MRad$.

3.2 Binomial distribution

If $\rho_{C_i}(q)$ is the probability distribution function for the charge injected into channel i, its comparator will have fired at time τ with the probability $p_i(\tau) = \int_{-\infty}^{\tau} \rho_{C_i}\left(\frac{k}{g}t\right) \cdot \frac{k}{g} dt$. Here g is the charge-to voltage gain and k is the slope of the voltage ramp.

If all C_i have the same distribution $(p(t))$ then, for a given time τ, the number of channels that have fired is described by the binomial distribution $N_\tau \in B(128, p(\tau))$. The probability that the counter will have started is $F(\tau) = P(N_\tau \geq D)$. The counter starting point distribution function is then $f(\tau) = \frac{\partial F}{\partial \tau}(\tau)$.

3.3 Charge distribution

Assuming that channels are independent, a family of charge distributions $(\rho_C(q))$ are generated. They are taken as mixtures of probability distributions: pedestal distribution, signal distribution and random noise. For instance, figure 5 shows a mix where 20% of the probability is spread out evenly as random noise, 60% of the probability is pedestal and the remaining 20% is in the signal. Thus the average signal occupancy is 20%. In a family of distributions the signal occupancy parameter is varied from 0% to 80%, while the noise remains at 20%. Each channel has an independent distribution, but they are all identical.

The signal peak is taken to lie 24,000 e^- above the pedestal peak. With the gain such that one ADC count equals 545 e^- that means 44 ADC counts. The distribution used had the pedestal peak at 80 ADC counts, and the signal peak at 124 counts. The width of the pedestal is 4 counts, the RMS width of the central part of the signal peak 6 counts. The pedestal is a gaussian distribution, the signal distribution is a parametrization of the measured SVX' signal distribution[3].

3.4 Statistical noise

The distribution of the counter start is calculated as a function of the DPS threshold (D) and the signal occupancy parameter. Figure 6 shows one such distribution as a dotted curve. Statistical noise is just the RMS width of the counter start distribution. In figure 7 the dotted curve shows this width as a function of occupancy in a family of distributions.

3.5 Efficiency

The solid curve in figure 7 shows the mean starting point for the ADC counter. The top panel of figure 8 shows the lowest signal needed to satisfy the sparsification cut when DPS has been taken into account. The sparsification threshold used is not the same for different DPS thresholds. Instead it is chosen so that

[3] F. Bedeschi *et al., Analysis of SVX Test Beam Data* (Pisa 1988).

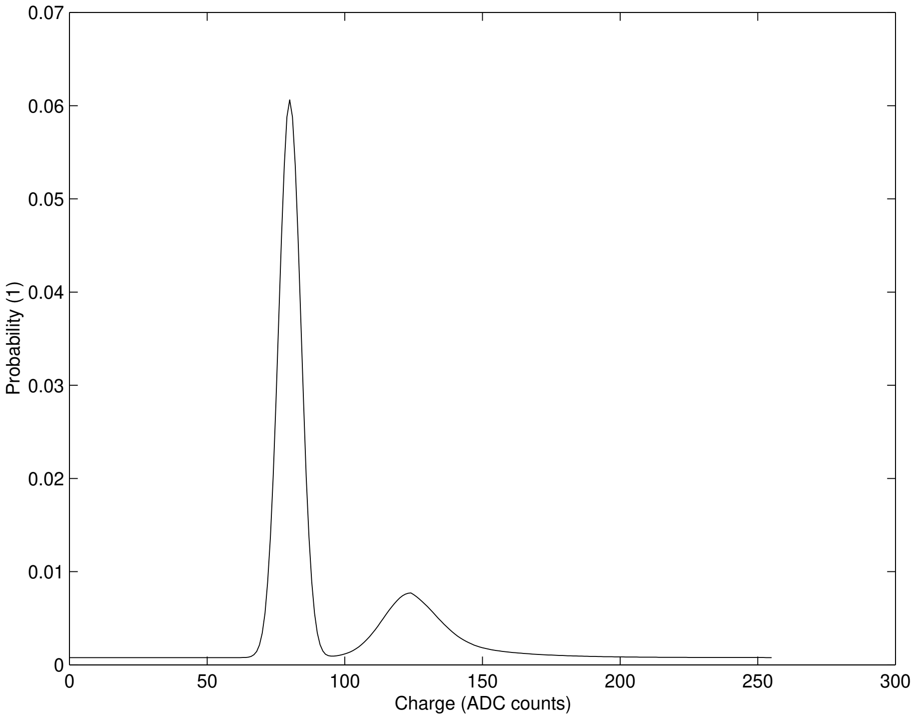

Figure 5: Example charge distribution: 60% pedestal, 20% signal, 20% noise.

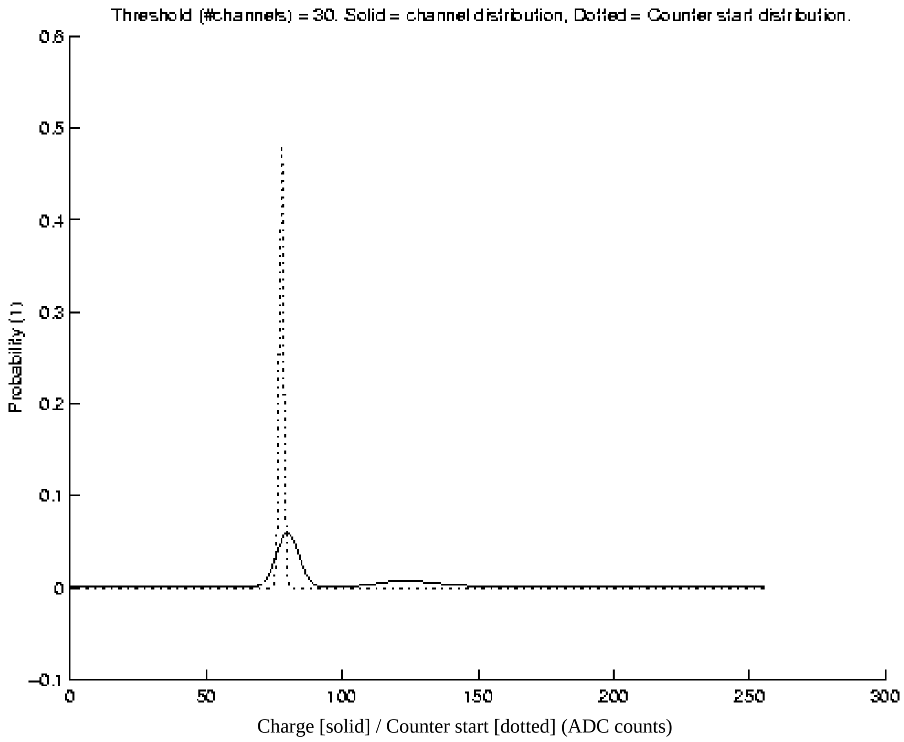

Figure 6: Counter start distribution for $D = 30$ superposed on figure 5.

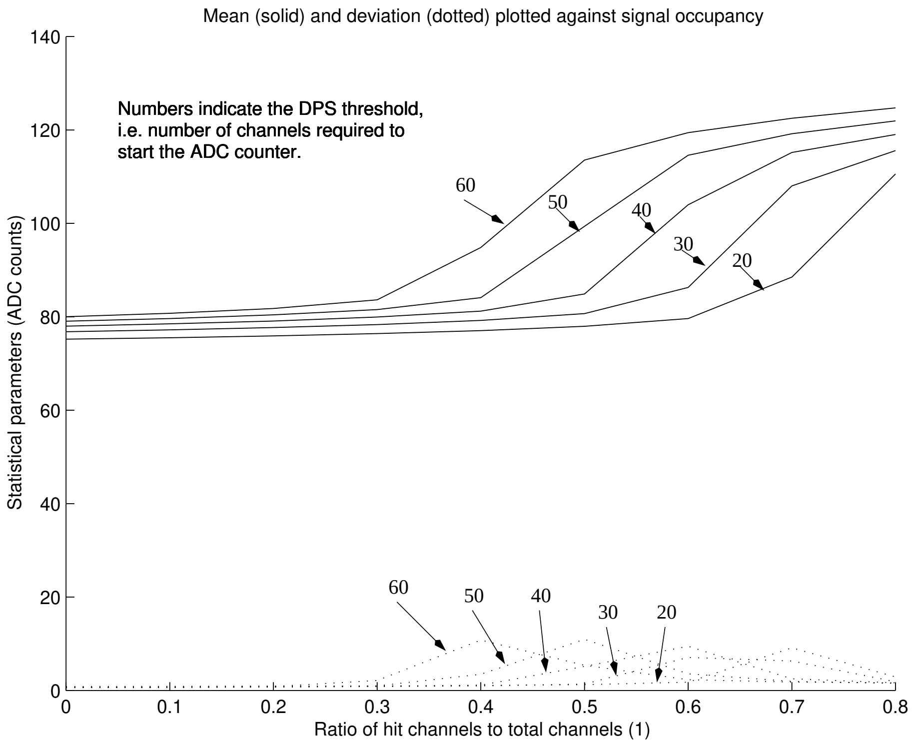

Figure 7: Statistical noise and displacement.

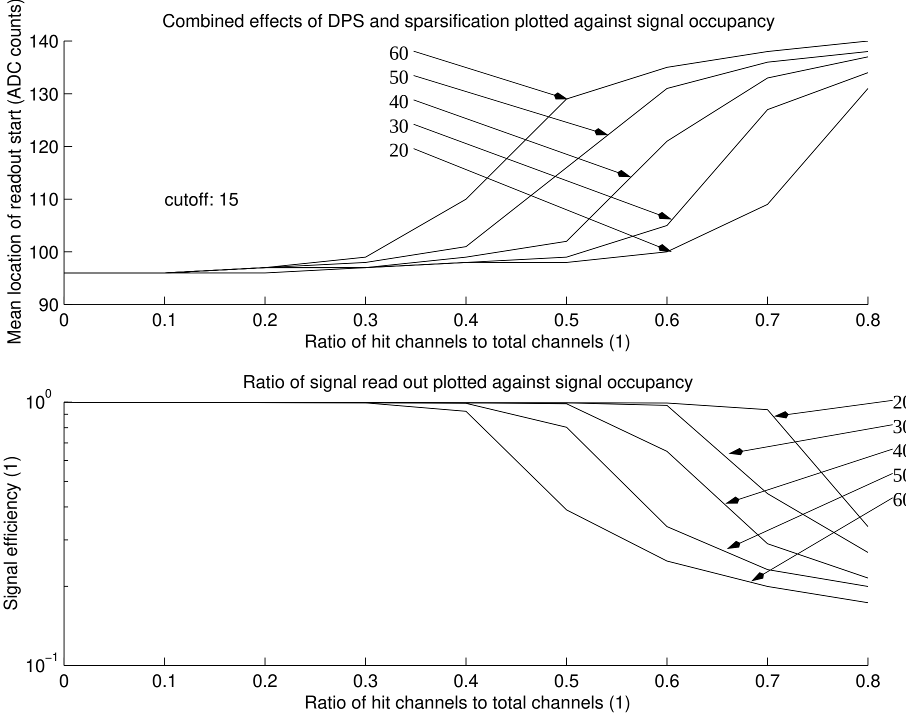

Figure 8: Combined effect of DPS and sparsification (top). Signal efficiency (bottom).

the sparsification cut occurs a certain number of counts above pedestal for a zero-occupancy chip. A higher DPS threshold will be combined with a lower sparsification threshold. That means that the curves coincide at occupancy zero, so that the shifting of the starting point can be directly compared for different thresholds. In the plot the sparsification cut at zero occupancy is 15 counts above pedestal (cutoff 15). The cases of 11, 15 and 20 counts were investigated. 11 counts correspond to $\frac{1}{4}$ of the signal–pedestal peak to peak difference.

The lower panel shows the efficiency: the fraction of signal channels successfully read out. The efficiency has been calculated using only the mean point of the counter start, disregarding any effect from the width of the counter start distribution in figure 6.

3.6 Noise occupancy from sloped pedestal

To calculate the noise occupancy generated by a sloped pedestal, a determininistic approximation is used. A deterministic distribution of channels was taken as the convolution of the individual channel's probabilistic distribution with zero signal and the slope.

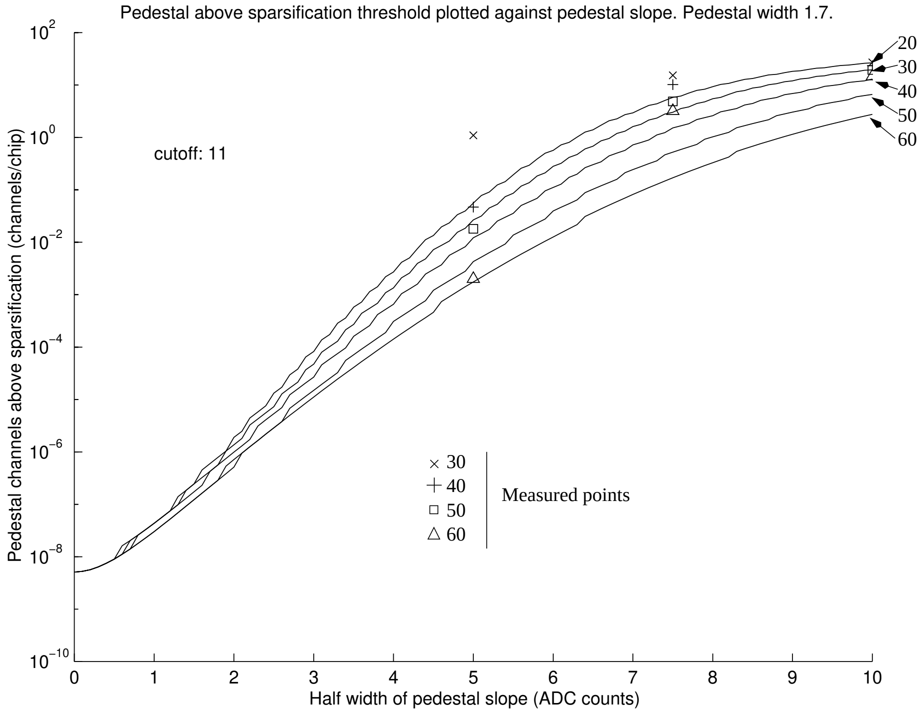

Figure 9: Noise occupancy. The noise occupancy problem is smaller for higher DPS thresholds and higher cutoff points. Numbers in figure label DPS thresholds.

For each DPS threshold, sparsification levels are calculated as described in section 3.5. This means that the performance at slope zero will be the same for all DPS thresholds as is evident from figure 9.

To calculate noise occupancy, counter start is taken to occur deterministically at the point where the integral of the channel distribution function reaches the DPS threshold. To find out the noise occupancy in readout the appropriate sparsification is added to that point. Noise occupancy is then simply the part of the channel distribution to the right of the location thus obtained.

In figure 9 the result for the worst case, a cutoff of eleven above pedestal, is shown together with experimental results. The latter were obtained using a broad laser pulse to mimic a sloped pedestal and are to be taken as very approximate.

Item	min	max
Chosen threshold	35	
Resistor tolerance	± 3	
Radiation	$+4$	
Actual threshold	32	42
Dead/Noisy channels	± 15	
Effective threshold	17	57

Table 1: Variation of DPS threshold level.

4 Results

4.1 Considerations

From the computations above the following measures were considered the most important:

1. Efficiency
2. Noise occupancy

Efficiency is maximized when using a low DPS threshold, noise occupancy is minimized by a high threshold.

The resistor–threshold function maps a manufacturing tolerance for the resistor into a variation of the threshold level. The radiation effects on that relationship will also contribute to changing the actual threshold value.

In addition there will be a certain number of noisy channels "dead low" and "dead high" channels in the input. Noisy channels are addressed in the calculations. A "dead low" channel's comparator will always fire immediately, thus effectively reducing the threshold level by one. A "dead high" channel will never fire. The combined effects (noise, dead channels, tolerance and radiation) give a window around a chosen threshold within which the effective thresholds will vary. Of course, performance must be good for the whole of that window. We therefore have to choose not one threshold value, but an interval of threshold values.

The manufacturing tolerance for the resistor is 10%. That means a variance of 3 channels in the threshold. The radiation induced shift translates into an increase in the threshold level by 4 channels during the operation of the SVX-II detector.

The effects are summarized in table 1. Note how critical the dead/noisy contribution is. The number of dead channel and noisy channels is hard to estimate at this early stage in production. Represented in the table is a rather arbitrary and pessimistic assumption.

Statistical noise	signal occupancy								
threshold	0%	10%	20%	30%	40%	50%	60%	70%	80%
30	0.70	0.73	0.78	0.86	0.99	1.38	7.09	6.33	1.88
40	0.64	0.69	0.75	0.87	1.15	5.16	9.48	2.50	1.65
50	0.62	0.68	0.77	0.99	3.46	10.97	3.58	1.97	1.57

Table 2: Statistical noise (ADC counts).

4.2 Choice of threshold

A resistor of 7 kilohm has been chosen, corresponding to a 35 channel DPS threshold. Statistical noise for the relavant threshold range is compiled into table 2. The signal efficiency can be read off from figures like 8. It has been tabulated for 30, 40 and 50 channels in table 3. Note that the 20% of noisy channels in the distribution (section 3.3) make actual occupancy higher than signal occupancy.

Noise occupancy from pedestal slope, as read off from figures like 9, is summarized in tables 4, 5 and 6. Figure 9 and table 4 show a low pedestal width in order to be comparable to the plotted measurements, which were done with a low-capacitance sensor connected (only one sensor, p-side). Tables 5 and 6 represent more realistic pedestal widths. The sparsification cuts vary depending on pedestal width. Therefore cutoff 11, slope 10 will give a smaller noise occupancy with a broader pedestal, contrary to what one could expect. The sparsification threshold is higher for the broader pedestal to achieve the same cutoff point. Put another way, the same slope is less important for a larger pedestal width.

The sparsification thresholds used to achieve the cutoffs in the computation are shown in table 7. They should give an idea on which sparsification levels to use in the chips with this gain, but will have to be modified according to the actual gain, pedestal width and number of noisy/dead channels. Again note the assumption about noisy channels used here.

5 Conclusion

5.1 Parameters

Statistical noise will be significant only for certain high occupancies, when counter start sometimes occur at pedestal, sometimes at signal. This occurs for instance with a DPS threshold of 50 channels and a signal occupancy of 50%. See figure 7. However, noise tolerance is relatively high in the tracking software with regard to the signal level. Precise knowledge of the gain is not critical to track reconstruction.

Signal efficiency drops rapidly at extreme signal occupancies. However, those will occur very seldom. Also the neighbor logic will resolve the problem to a large degree. Nevertheless it must be considered an important parameter.

30 channel DPS threshold

Signal Efficiency	signal occupancy				
cutoff	40%	50%	60%	70%	80%
11	100%	100%	99%	58%	36%
15	100%	99%	97%	45%	27%
20	98%	98%	92%	31%	19%

40 channel DPS threshold

Signal Efficiency	signal occupancy				
cutoff	40%	50%	60%	70%	80%
11	100%	100%	78%	39%	29%
15	99%	99%	65%	29%	21%
20	98%	96%	48%	20%	15%

50 channel DPS threshold

Signal Efficiency	signal occupancy				
cutoff	40%	50%	60%	70%	80%
11	100%	89%	45%	31%	27%
15	99%	80%	34%	23%	20%
20	97%	65%	23%	16%	14%

Table 3: Signal efficiency. 100% means $\geq 99.5\%$.

30 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.00	0.00	0.28	5.47	19.54
15	0.00	0.00	0.00	0.04	1.92
20	0.00	0.00	0.00	0.00	0.00

40 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.00	0.00	0.11	2.60	13.04
15	0.00	0.00	0.00	0.01	0.59
20	0.00	0.00	0.00	0.00	0.00

50 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.00	0.00	0.04	1.03	6.64
15	0.00	0.00	0.00	0.00	0.10
20	0.00	0.00	0.00	0.00	0.00

Table 4: Noise occupancy (channels/chip). Pedestal width 1.7 ADC counts.

30 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.04	0.28	1.67	6.75	16.32
15	0.00	0.00	0.05	0.56	3.11
20	0.00	0.00	0.00	0.00	0.07

40 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.04	0.23	1.26	4.78	12.22
15	0.00	0.00	0.03	0.32	1.84
20	0.00	0.00	0.00	0.00	0.03

50 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.04	0.21	0.94	3.45	8.75
15	0.00	0.00	0.02	0.19	1.02
20	0.00	0.00	0.00	0.00	0.01

Table 5: Noise occupancy (channels/chip). Pedestal width 3 ADC counts.

30 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.54	1.30	3.55	8.27	16.26
15	0.02	0.08	0.36	1.39	4.37
20	0.00	0.00	0.01	0.05	0.33

40 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.51	1.23	2.92	6.87	13.01
15	0.02	0.07	0.28	1.06	3.12
20	0.00	0.00	0.00	0.03	0.19

50 channel DPS threshold

Noise occupancy	pedestal half slope				
cutoff	2	4	6	8	10
11	0.51	1.16	2.65	5.65	10.30
15	0.02	0.07	0.24	0.79	2.16
20	0.00	0.00	0.00	0.02	0.11

Table 6: Noise occupancy (channels/chip). Pedestal width 4 ADC counts.

Sparsification threshold	cutoff		
DPS threshold	11	15	20
30	14	18	23
40	13	17	22
50	12	16	21

Table 7: Sparsification thresholds (ADC counts).

Readout of one channel takes $20\,ns$. Readout of a ladder we assume at this time must be completed in $20\,\mu s$, allowing 1000 channels. The largest SVX II ladder has 14 chips, which means the maximum occupancy per chip, including channels added by neighbor logic, is 70 channels. It is important to realize that typically not all chips will be equally affected by slope. Some may at one time be severely affected by pickup, while others have negligible slope. Equally important: all numbers given in the tables are calculated disregarding the neighbor logic. With neighbor logic turned on, in the best case one channel should be added to the occupancy. In the worst case the noise occupancy should be multiplied by three! The best case will be realized if the affected channels are in sequence, the worst case if they are scattered randomly across the chip.

5.2 Further investigations

A more ambitious approach to conduct this investigation would be to use a real Monte Carlo simulation of physics events. Such a simulation could address the issue of neighbor logic in a more realistic way. On the other hand it would not improve control over important factors such as electromagnetic pickup and sensor defects.

Left to investigate is in what numbers bad channels will occur in the finished sensors and what their characteristics are. The external resistors produced (nominally $7\,k\Omega$) have not all been measured. More chips, both irradiated and non-irradiated could be tested to check for variations in the resistor–threshold function.

5.3 DPS usefulness

It has been shown here that it is indeed possible to find settings such that dynamic pedestal subtraction works satisfactory. DPS has proven to be an essential tool in managing common mode noise in practical tests[4].

[4] M. Garcia-Sciveres *et al.*, *The SVX3D Integrated Circuit For Silicon Strip Readout* (CDF note 4851).