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Radiation Effects on the SVX3 Chip

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Abstract

We irradiated SVX3 chips with gamma rays from a cobalt source to study their tolerance to ionizing radiation. The SVX3 chip is the custom integrated circuit that will be used to read out the sensors of the SVXII silicon vertex detector. After 3.5 Mrad(Si), we observed only small changes due to radiation and concluded that the chip will remain operational during all of Run II.

[1]Visitor

1 Introduction

The purpose of this study was to investigate the effects of radiation on the SVX3 chip, which is the integrated circuit that will be used to read out the SVXII detector [1]. The prototype chips irradiated were fabricated by Honeywell in their 0.8μm CMOS radiation-hard bulk process.

Radiation can cause damage by two mechanisms. It can break atomic bonds creating free charge that can accumulate in electrical insulators (ionization), or it can scatter off atomic nuclei giving rise to defects in crystal lattices (bulk damage). In MOS devices bulk damage is negligible in comparison with ionization damage [2] because defects in the silicon lattice primarily affect the relatively unimportant minority carriers, whereas charge accumulation in the oxide layers can significantly alter transistor properties. Note that the situation is very different for silicon sensors, where bulk damage is the primary concern.

During Run II the chip will be exposed to about $7 \cdot 10^{13}$ minimum ionizing particles per cm^2 over a period of two years, corresponding to an absorbed dose of 2 Mrad [3]. This is the dose expected for the parts closest to the beam. The irradiation for this study was done with a Co^{60} gamma ray source as is commonly used in industry. The source delivers photons at 1.17 MeV and 1.13 MeV. A 1.1 MeV photon does not have the same effect as a minimum ionizing particle, but the chip was exposed to radiation delivering an ionizing dose equivalent to the particles in Run II. No appreciable bulk damage is caused by the exposure to gamma rays.

2 Dosimetry

To investigate the characteristics of the source, measurements were made using thermoluminescent dosimeters. A first series of measurements of the dose at different distances from the source (fig: 1) revealed that to reach 2 Mrad within a reasonable time, the chip had to be positioned as close to the source as possible.

A metal fixture was constructed to hold the chip in the same position at every irradiation, as small differences in distance from the source would result in large dose variations. This distance was fixed by the fixture to 14 cm ± 2 mm. A second series of measurements was now made to determine the dose rate the chip would receive at this position (fig: 2). The average

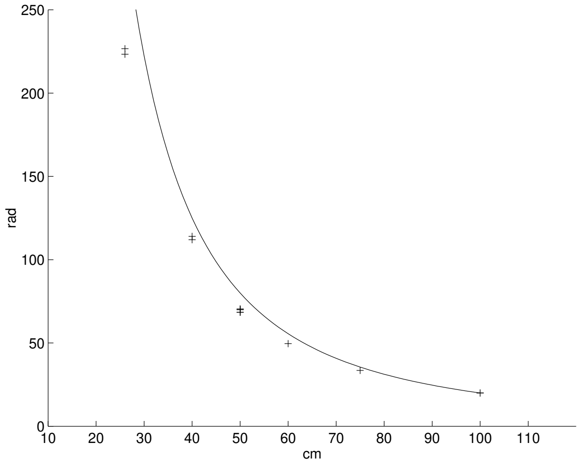

Figure 1: *Absorbed dose vs distance from source. The solid curve is that of a ideal point source giving the same dose at 1 m.*

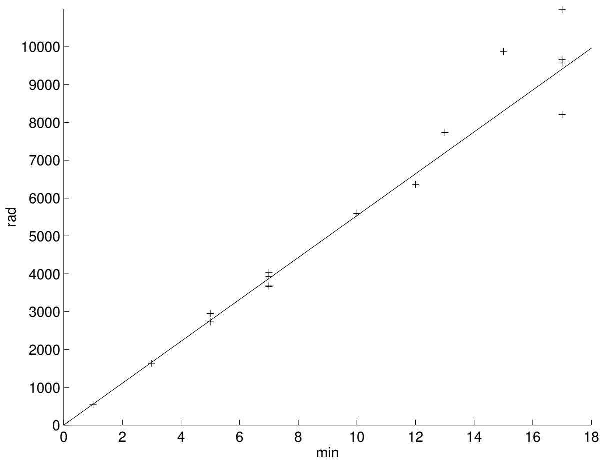

Figure 2: *Dose as function of time at chip position.*

rate turned out to be 554 rad/min with an RMS error of 51 rad/min or 9%.

As the dosimeters are not made out of silicon, the dose they absorb will not be the same as that received by the chip. To relate the dose absorbed by two materials exposed to the same radiation, one needs to assume that there is charged particle equilibrium (CPE) [2] defined as a state in which the energy carried into a volume by electrons equals that carried out by electrons. Under CPE, the only net energy deposit in the material is transferred directly from photons to the material. If CPE is established, the absorbed doses relate as the mass energy absorption coefficients (μ_{en}/ρ) of the materials. These coefficients have been tabulated [4] for a large range of materials and photon energies. In our case, we had to take into account that in addition to the primary photons of the wavelengths mentioned above, Compton scattering inside the source and on the walls generates photons with a peak [2] around 0.2 MeV. Measuring the absorbed dose with several kinds of attenuators with different μ_{en}/ρ made it possible to estimate that these rays were responsible for about 11% of the energy deposited in the dosimeters. The TLDs used in these measurements are made out of lithium borate crushed powder ($Li_2B_4O_7$:Cu) which is made to resemble human tissue. The mass energy absorption coefficient of tissue was used lacking that of the TLDs. For photons of 1.25 MeV and 0.2 MeV, we have $(\mu_{en}/\rho)_{Si}/(\mu_{en}/\rho)_{Tissue} = 0.903$ and 0.987 respectively. Weighted with the fraction of each photon energy, we get a conversion factor of 0.912 between dose measured by the TLDs and the dose absorbed by the silicon. This gives us a dose rate of 505$\pm$46 rad(Si)/min. In the following text, all doses will be given in rad(Si) taking this factor into account. To try to achieve CPE, which is necessary for the conversion factor to be accurate, the chip was placed with the board, containing high atomic number materials (as gold), towards the source. An additional 1 mm of aluminum, which has a mass energy absorption coefficient close to that of silicon, was also glued between the chip and the test board.

Near material interfaces the discontinuity in μ_{en}/ρ can cause CPE to be lost leading to dose enhancement effects. For 1.2 MeV photons, the maximum enhancement following a gold–silicon interface is 20%, but the effect may be significantly higher for low energy photons leading to a potential uncertainty. However, since a large error times 11% is small compared to other uncertainties, we conclude that it would not be necessary to filter out the lower energy rays.

Finally, the dose rate during the irradiations with Co^{60} is much higher than what the chip will be exposed to during Run II. In MOS devices, a low dose rate can be simulated by a high rate followed by appropriate annealing [5]. To achieve this, after reaching full irradiation, the chips were left to anneal at 100 $^{\circ}$C for a week. Measurements of the chip properties were made both before and after annealing as proposed by reference [5] in order to be sure of measuring stronger radiation effects than what can be expected during normal operation with low dose rate [6].

3 Test Conditions

During all exposures, a black cloth assured that the chip was held in darkness. The chip was not cooled but did not get much hotter than room temperature. To simulate the existence of a detector, some channels were loaded with 10 pF and 22 pF input capacitors.

Electric fields in the oxide are an integral part of the radiation damage mechanisms in MOS devices and so operating the electronics during irradiation is crucial for realistic radiation damage. During our tests, the chips were powered and operated during exposure using the PATT chip test setup [7] implemented with a personal computer. As computer and power supplies had to be put behind a protective wall 6 m from the source, voltage regulators near the chip held the voltages at 5 V for DVDD and AVDD. AVDD2 was set to 3.5 V. PATT board and regulators were protected by lead bricks. Running the chip during exposure also permitted us to monitor it continuously and perform some tests. The irradiations typically went on overnight. About every half hour, a series of measurements was made. The sequence of operation of the program running the chip was:

1. Tests are performed for about seven minutes to measure RMS noise, rise time, leakages and pedestal uniformity.

2. In-between test cycles, that is for about 20 min, a dummy program is run. This program injects charge in some channels and then reads out the chip each time using a different cell. It is built up as:

    - A pattern with main blocks: initialization, acquisition, digitization and readout which takes 80 μs.

    - During the remaining of a millisecond, the chip is powered, but with all control signals fixed.

The board operating the chip used a 50 MHz clock and a 140 ns beam structure.

4 Test Results

Three chips were irradiated to doses of 3.5, 4, and 2 Mrad(Si) respectively. Results are shown for the 3.5 Mrad(Si) chip as long as the data from the other chips are consistent. Some of the measuements done on the 3.5 Mrad(Si) chip were repeated on only one of the other two chips (for example the digital output delay measurements). All chips under test continued to operate at full speed after the complete exposure. Some details of the chip response did change with dose and we touch upon these with particular attention to those affecting the signal to noise performance.

The preamp gain (5 mV/fC) is given by the value of the feedback capacitor (200 fF) as long as the open loop gain is high and is therefore not expected to change with radiation. However, the measured gain is that of the full data path from preamp to ADC and as shown in figure 3, the gain increases with dose by about 15% (on average, the gain is roughly 1/697 ADC/electron). The increase could be due to a slow-down of the ADC ramp. Figure 4 shows a decrease with dose of the back end ramp rate voltage, which controls the ADC ramp. The source of this voltage is the diode in a current mirror that goes to an external resistor used to set the ramp current. As transistor thresholds shift, the ramp rate voltage should therefore show the same behavior. Such a slow-down of the ADC ramp would also lead to a pedestal shift with the same dose dependence as can be seen in figure 5. When corrected for the variation of the gain, the pedestal remains stable at the 10% level (fig: 6).

Single-channel noise is measured as the RMS of ADC counts using the chip ADC conversion. However, we show noise in electrons after correcting for gain. The noise level is seen to increase (fig: 7) with dose and also to change with annealing. It would not be unreasonable to expect a 20% increase in noise after 2 Mrad. The largest deviation measured is 40%. These figures are conservative as no common-mode subtraction or filtering of non-Gaussian tails of the ADC distribution were performed.

Effects leading to pedestal shifts between different events can increase the effective noise. Leakage in the pipeline capacitor switches can potentially cause such shifts. This effect was observed after the first irradiations. It was investigated by leaving the pipeline capacitors idle for different amounts of time before digitization and readout. The effect was measurable only for times of the order of a millisecond while normal operation is expected to allow pauses of at most 50 μs. As a representative case, the rate of pedestal shift due to leakage in the reference capacitor of one channel is given as function of dose in figure 8. The largest rate of shift observed, 25 counts per millisecond, would lead to a mere 1 count shift after 50 μs.

Pedestal non-uniformity also adds to effective noise as there is only one sparsification threshold per chip. To measure this non-uniformity, the data taken on-line for each pipeline cell and channel were used to compute a pedestal distribution. A Gaussian was fitted to the distribution and figure 9 shows the variation of its σ with dose. This width is a measure of the scatter of the mean pedestal in all cells and channels about a global average pedestal, whether random or due to a systematic shift with channel number and/or cell number. Though varying, the width of the pedestal distribution stays below 2.5 counts and 2-dimensional plots of the pedestal for all cells and channels show no obvious systematic variations. Since the observed variation is not monotonic, it may be due to radiation damage or to something else such as a source of common-mode noise.

The front end preamplifier reset voltage is a direct measure of the threshold voltage of the input transistor. As seen in figure 10 the change in voltage is in relatively good agreement with the data provided by the chip manufacturer, Honeywell. The offset level of the data points from Honeywell has been chosen to fit our data.

Selected bias voltages were measured and, as can be observed in figure 4, vary with slopes of absolute value between 0.7 %/Mrad(Si) and 3.4 %/Mrad(Si). These do not have any simple interpretations but drastic changes would have raised a warning flag that needed to be investigated further. The measured DC currents (fig: 11) do not seem to change more than about 20%. As a result, power dissipation should not increase in such a way as to justify adjustment of cooling systems with increasing dose.

The propagation delays between edges of different digital output signals were measured. Unfortunately, the data from two different chips are not in good agreement (figs: 12 - 15), and it is possible that much of the disagreement is due to systematic biases in the measurements. For example, the oscilloscope probes used did not all add the same delay, and they may have been swapped in between measurements. In the absence of systematic biases, any shift with dose of the double difference "back end clock" to "data valid" delay minus "back end clock" to data bit delay will indicate a decrease in setup and hold time margins. A large shift could be compensated at the data receivers, but that would require re-tuning timing in hardware with increasing dose. The data points have a substantial scatter, but on average, one of the chips shows no relative shift between "data valid" and the data bits (figs: 12,13), whereas the other chip shows a 1-3 ns shift per Mrad(Si) (figs: 14,15).

Rise time plots for the input transistor were made on-line for different bandwidths. No noticeable dose dependence was observed. Figure 16 shows the plots for one channel at different dose levels for maximum bandwidth.

5 Errors

The dominant uncertainty in this study comes from the dosimetry. In section 2, various sources of error were mentioned that can be found combined in table 1. We have assigned a 10% error to possible lack of CPE based on data for dose enhancement effects near interfaces [2] for the 1.25 MeV rays and 30% for the 0.2 MeV ones.

Source	*Error*
TLD Dose measurement	9%
Chip positioning	3%
Charged particle equilibrium*	9%
Low energy gamma rays*	3%
Total error	15%

Table 1: *Errors connected with dosimetry. $*$ marks correlated errors.*

Note that with the exception of figure 9, all figures lack error bars. The figures with data taken on-line are based on large event samples leading to negligible statistical errors. The equipment used to measure voltages and currents has negligible measurement errors. The propagation delays (fig: 12 and 13) on the other hand, have a ± 1 ns measurement uncertainty and the procedure used to define edge crossings varied during the study contributing an additional 2-3 ns systematic uncertainty. No error bars are shown for the delay points, but the observed scatter is indicative of these uncertainties. The points may have additional systematic biases as discussed in the previous section.

The uncertainty concerning the gain, and therefore also the noise, is dominated by our knowledge of the SVX3 internal calibration capacitance which carries a 10% error. This is a correlated systematic uncertainty which affects normalization of plots but not their shape vs. dose.

6 Conclusion

After irradiation up to 4 Mrad(Si), the SVX3 chips that were tested continued to work at full speed. The features that are affected by the dose experience changes that should not cause problems for the operation of the chip during Run II. No adjustments of equipment with increasing dose should be necessary, with the possible exception of the timing in the data receivers, where the results obtained can neither support nor rule out this possibility. Further study is clearly needed to settle this question, but it should be pointed out that some signals have critical timing within the chip for the version tested here, and so it is possible that the inconsistent behavior is real. It would therefore be best to revisit the effects of radiation on data delays using the next version of the chip.

The rise in gain will require tuning of the sparsification threshold level. The observed gain variations will affect pedestal and signal equally. As mentioned earlier, noise can be expected to rise by about 20% when approaching 2 Mrad, affecting the signal-to-noise ratio by the same amount since there is no observed change in the bandwidth.

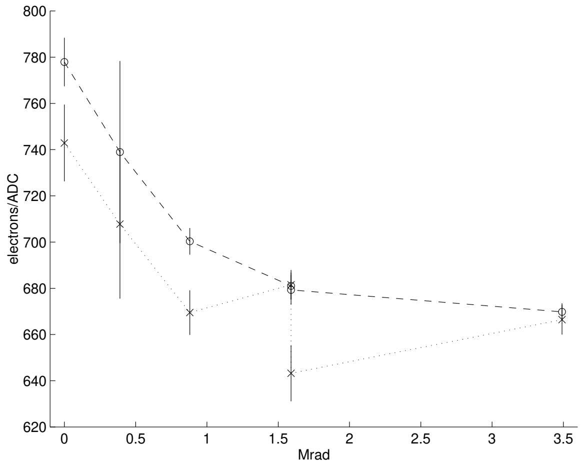

Figure 3: *Inverse gain for a channel without capacitor (dashed line) and a channel loaded with a 10 pF capacitor (dotted line).*

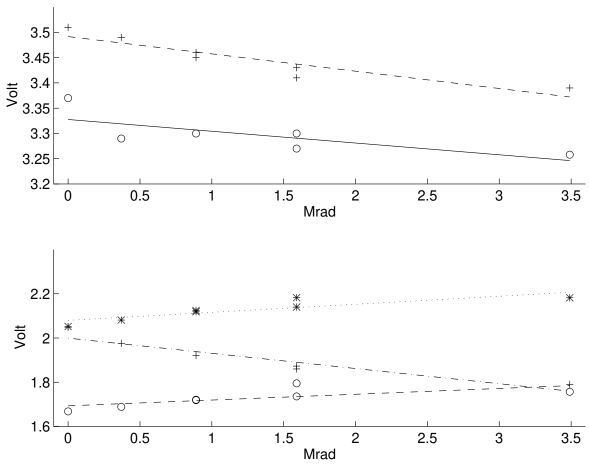

Figure 4: *DC voltages vs. dose. Upper plot – BE I drivers: ∘ and solid line. FE Iset 2: + and dashed line. Lower plot – FE Iset 1: ∘ and dashed line. BE Iquiecent: ∗ and dotted line. BE Ramp rate: + and dot–dashed line.*

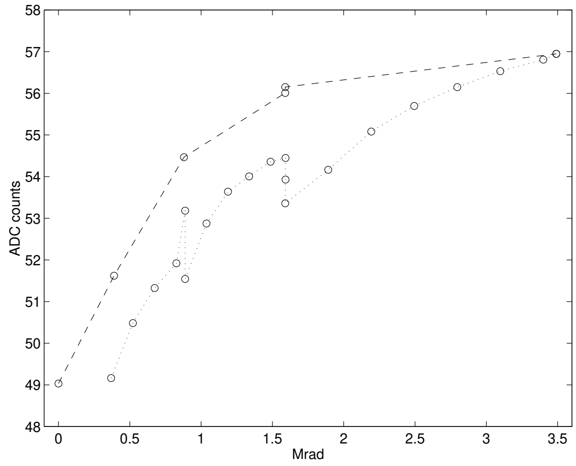

Figure 5: *Dotted line: Average pedestal over all cells and channels vs. dose. Dashed line: Gain (ADC/charge) normalized to the pedestal maximum value. More than one point at the same dose indicates that annealing took place between them. Points are connected in order of increasing time.*

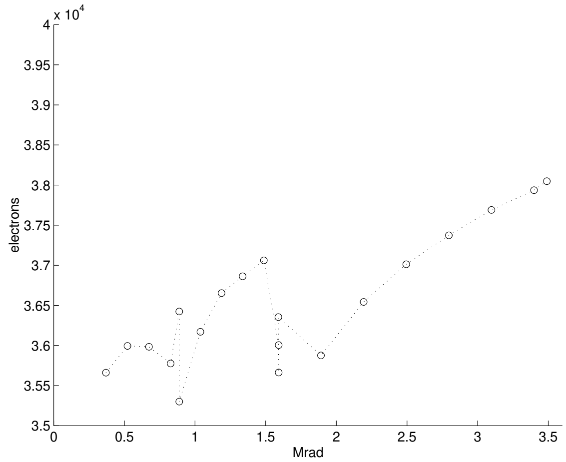

Figure 6: *Pedestal* $\times$ *gain for two channels vs. absorbed dose.*

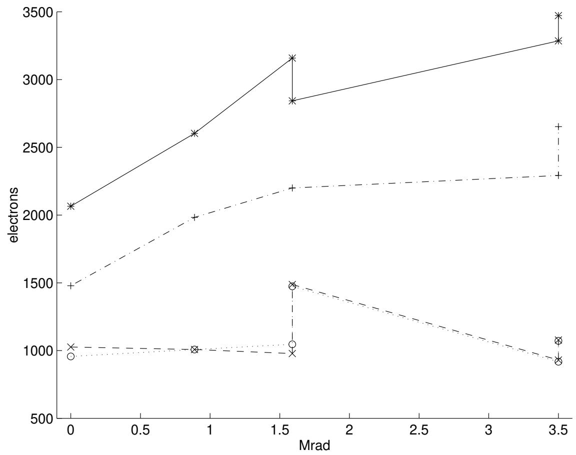

Figure 7: *RMS noise vs. absorbed dose for two channels without capacitor ($\circ$ & $*$), one channel loaded with a* 10 *pF capacitor ($\times$) and one loaded with* 22 *pF (+). More than one point at the same dose indicates that annealing took place between them. The points are connected in order of increasing time. We used bandwidth setting of 3 and integration time of* 120 *ns.*

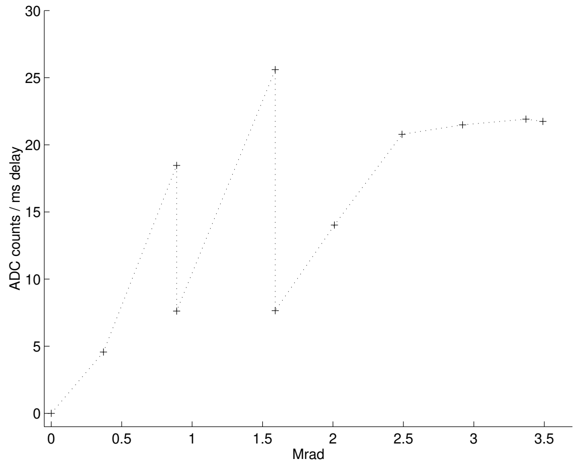

Figure 8: *Rate of pedestal shift due to leakage of the reference capacitor of one channel as function of absorbed dose. More than one point at the same dose indicates that annealing took place between them. The points connected in order of increasing time.*

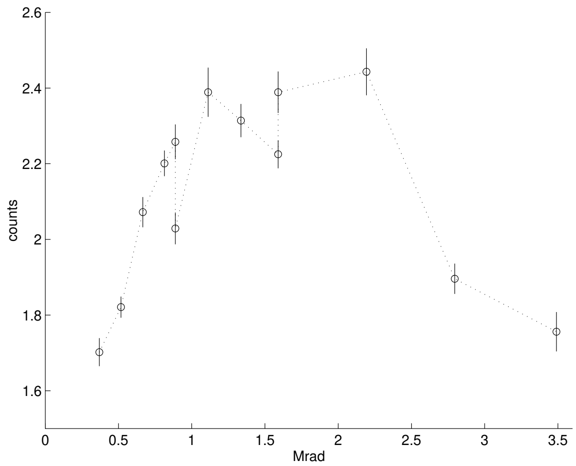

Figure 9: *σ of Gaussian fits to the distribution of counts for the pedestal of all channels and cells vs. absorbed dose.*

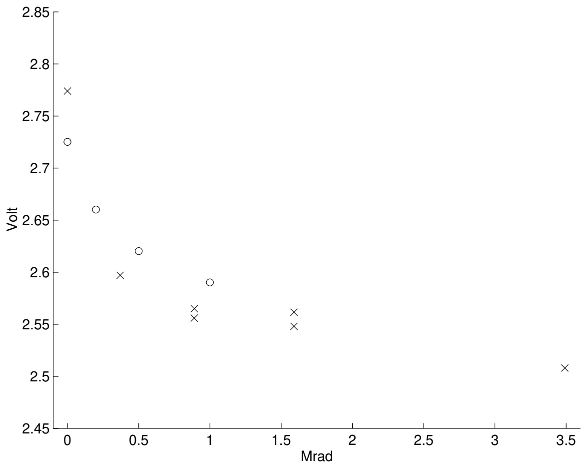

Figure 10: *Front end preamp reset voltage ($\times$) and data from Honeywell [8] ($\circ$) vs. dose. The first point is high compared with data from other chips. Honeywell data is for pmos transistor threshold shift with an added DC offset.*

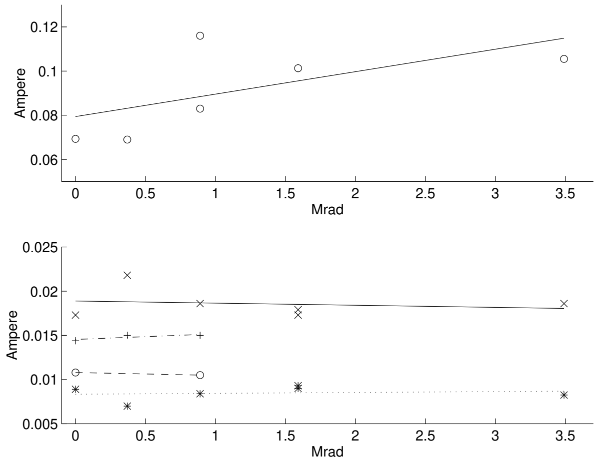

Figure 11: *DC currents vs. dose. Upper plot – AVDD total. Lower plot – AVDD 2:* $\times$ *and solid line. Preamp AVDD:* $\circ$ *and dashed line. Back End DVDD:* $*$ *and dotted line. Back End AVDD + QVDD:* $+$ *and dot–dashed line.*

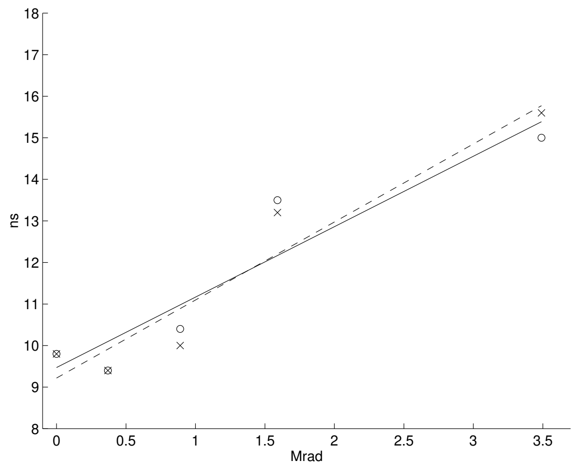

Figure 12: *Chip A delay between back end clock and data valid vs. dose. Rising edge to rising edge:* $\circ$ *and full line. Falling to falling:* $\times$ *and dashed line.*

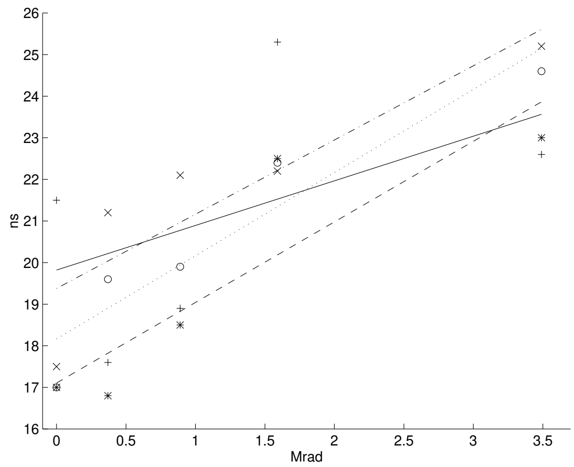

Figure 13: *Chip A delay between back end clock and data bit zero vs. dose. Rising edge to rising edge:* $\circ$ *and dotted line. Falling to falling:* $*$ *and dashed line. Rising to falling:* $+$ *and full line. Falling to rising:* $\times$ *and dot–dashed line.*

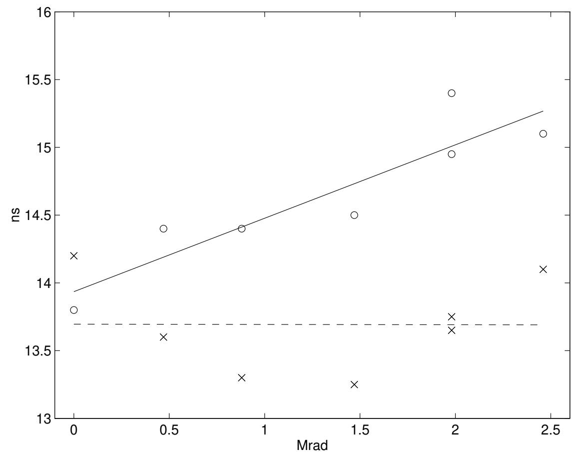

Figure 14: *Chip B delay between back end clock and data valid vs. dose. Rising edge to rising edge:* $\circ$ *and full line. Falling to falling:* $\times$ *and dashed line.*

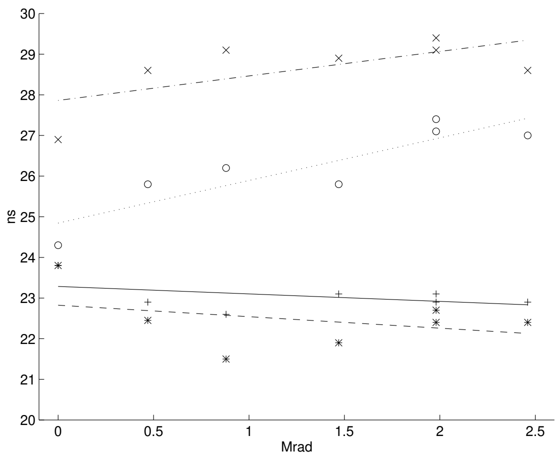

Figure 15: *Chip B delay between back end clock and data bit zero vs. dose. Rising edge to rising edge:* $\circ$ *and dotted line. Falling to falling:* $*$ *and dashed line. Rising to falling:* $+$ *and full line. Falling to rising:* $\times$ *and dot–dashed line.*

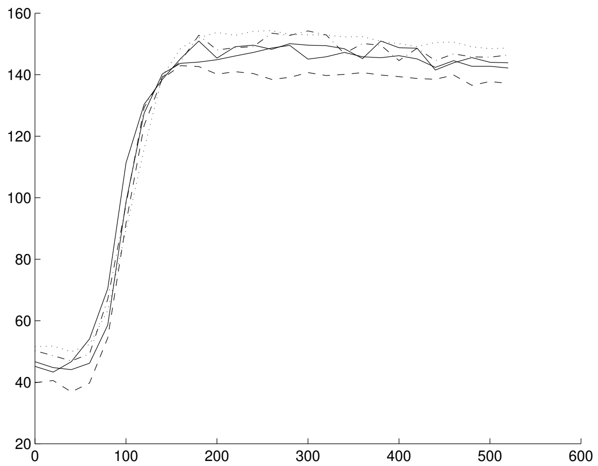

Figure 16: *Rise time plots of the input transistor for a channel loaded with a* 10 *pf capacitor for doses ranging from* 0.3 *Mrad(Si) to* 3.59 *Mrad(Si) with bandwidth setting* 7.

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[6] **Note:** Dose rate is an issue for bipolar devices but not for MOS technology. See eg. [5].

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