Master's Thesis

The Effects of Ionizing Radiation on the SVX3 Chip

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TRITA-FYS-9022

CONTENTS

ABSTRACT

A system for irradiating SVX3 readout chips of the SVX II detector with gamma rays to test their dose hardness is described. The dosimetry aspects of the study are thoroughly treated. Some background is given about the theory of radiation effects on electronics. Further, a test scheme for the radiation effects is presented focusing especially on features affecting the signal-to-noise relation. The observed effects are quantitatively described and explained to the degree they are understood.

ACKNOWLEDGMENTS

First of all, I would like to thank Maurice Garcia-Sciveres for guiding me through this work. I also express my sincere gratitude to the rest of the CDF group at LBL for making me feel welcome and especially Igor Volobouev and Robert Ely who played important roles in the study. Thanks to my supervisor Per Carlson who made it possible for me to come to California. Finally I would like to thank all the people I knew in Berkeley and El Niño who, in different ways, made my stay unforgettable.

1 BACKGROUND

1.1 INTRODUCTION TO THE PROJECT

The CDF group of the physics department at the Lawrence Berkeley National Laboratory (LBL) presently works on a new version of the silicon vertex detector (SVX) that has been used in the Collider Detector at Fermilab (CDF). During its use, the new detector (SVX II) will receive large doses of radiation. The purpose of this study was to test the dose hardness of the SVX3 chip which is the integrated circuit used for data readout from the silicon strips. The study was done at LBL during the period September 1997 – February 1998. The results were briefly presented in a CDF-note [1].

1.2 THE TEVATRON

The Fermilab Tevatron collider at Batavia near Chicago is presently the world's highest energy particle accelerator and will remain so until LHC at CERN is put into operation in the middle of the next decade. The Tevatron was designed for the study of $p\bar{p}$ collisions at energies of up to $\sqrt{s} = 1.8$ TeV (see A.1.2) with integrated luminosity (see A.1.1) increasing gradually from 25 nb^{-1} in 1987 to 90 pb^{-1} in 1994. The first events were registrated in 1985 but the accelerator was really set into operation first in 1988 during Run 0 (1988-1989). Following runs were named Run 1a in 1992-1993 and Run 1b in 1994-1996. During this last run, instantaneous TeV luminosity of more than $2 \cdot 10^{31}$ cm^{-2}s^{-1} was reached. There are two experiments at the Tevatron at the points of collision of the circulating p and $\bar{p}$; The Collider Detector at Fermilab (CDF) and Dzero (DØ) named after its position around the accelerator. Each of these experiments is composed of several detectors wraped around each other as the layers of an onion.
At the moment, the Tevatron is undergoing upgrading work for the planed Run II which is to start sometime during year 2000. The stated goal is to attain luminosity of up to $2 \cdot 10^{32}$ cm^{-2}s^{-1} with 2 fb^{-1} at $\sqrt{s} = 2$ TeV. The energy increase is relatively small but significant to increase $t\bar{t}$ production. What really influences the construction of the detectors are the luminosity and the time between crossings of particle bunches. During Run II, crossing times will be either 396 ns with 36 bunches or 132 ns with 108 bunches circulating the accelerator. This sets high expectations on the speed of operation of the different detectors and their data acquisition systems.
The Tevatron received much publicity in march 1995 when the CDF collaboration published an article announcing the discovery of the top quark [2].

1.3 TOP – ELUSIVE PARTICLE FOUND IN ILLINOIS

The observation of the top quark by the CDF collaboration in march 1995 marked the end of a hunt that had been going on since the bottom quark was found at Fermilab in 1977. The last elementary particle of the standard model* had now been observed. For almost two decades, no direct evidence of top existance had been found. The lower limit of its expected mass was slowly pushed further and further up as experiments with higher and higher energy failed to find the sought quark. When the top was finally found, its mass was measured to the unexpectedly high $m_t = 176.8 \pm 6.5$ GeV, roughly the weight of an atom of gold.

1.3.1 Searching Odds

To find the top quark, the first requirement was to produce it. Theoretically, 353.6 GeV of energy concentrated in a tiny volume would be enough to create a $t\bar{t}$ pair. The problem is that when $p\bar{p}$ collide at such high energies, the acting particles should be seen as a cloud of gluons and quarks. The energy must therefore be such that two colliding quarks or gluons have a reasonable probability of carrying at least 353.6 GeV

*Described briefly in appendix A.2

and so TeV energies are sought. However, the most probable if this energy is obtained is the production of a pair of lighter quarks or maybe gluons. These are odds that are hard to beat but by making enough attempts you might succeed. In the tevatron, the protons and antiprotons are circulating in bunches of about 10^{11}particles and the bunch collision frequency was in the previous runs $3 \cdot 10^5$ s^{-1} which is also be the average frequency of interactions. During the first run, 10^{12} events were stored on tape and about 100 tops were expected. At 1.8 TeV, the cross section for top production is about 6 pb, far less than the cross section for most other inelastic interactions making the difficulty with detecting the top mainly a question of separating the few interesting interactions from the very many uninteresting ones. The CDF detector is quite performing when it comes to caching and identifying the debris from a $\mathrm{t\bar{t}}$ collision but there is many orders of magnitude more of background that has to be filtered out. Many events look just like a top even after quite close scrutiny. As described more precisely below, W-bosons are plentifully produced in $\mathrm{t\bar{t}}$ interaction and even the cross section for getting a W from a non-top event is about twice that of the top. The necessary way to go is the following. The detector is constructed to look for events with typical top signatures. A certain number of them are registrated. After this, one has to calculate the expected background and compute the probability that the background could fluctuate up to the registrated number. With large statistics, this method could work but as mentioned earlier, the expected number of tops in Run I was 100 and far from all of them will be identified. This is were the SVX and so called vertexing comes in. Before describing this method, a short overview of the decay modes of the top is necessary.

1.3.2 Top Decay

The top quarks produced in $p\bar{p} \longrightarrow t\bar{t}$ have a life time of 10^{-24} s and so will never be directly observed. However, identifying its decay modes permits to see the traces it leaves. The dominant top decay is

$$\begin{aligned} t &\longrightarrow W^+ b \\ \bar{t} &\longrightarrow W^- \bar{b} \end{aligned} \tag{1.1}$$

The W boson has very short life time as well and immediately decays into either quarks giving rise to jets, or a lepton and antineutrino. The top events can therefore be classified according to decay mode into the categories: dileptonic (both W bosons decay leptonically), lepton + jet (one W decays into leptons and the other into quarks) and jets (both W go to jets). As many other processes not involving a top can mimic these decays, it is important to calculate the expected backgrounds due to these cases. Top production will then be indicated by an excess number of such events. The most easily identified events (dileptonic) are the rarest and the most plentiful (jets) have the biggest background. In the first run, the existence of the top was based on all in all 56 events out of the 10^{12} (see table 1). Three methods for identification of top events were used:

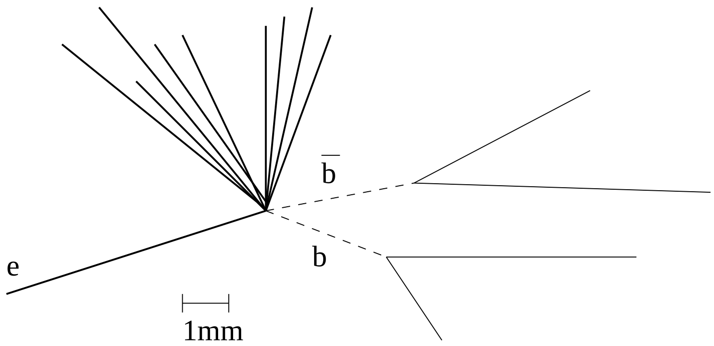
- Straight forward identification of dileptonic decay.
- Identification of lepton + jets decay with b-quark tagging by means of the SVX (see 1.3.3).
- Identification of lepton + jets decay with b-quark tagging finding additional leptons from the b decay.

Combining the findings listed in table 1, CDF found that the observed events were not consistent with expected background to 4.8 σ deviation in a Gaussian distribution or a combined probability of 10^{-6}. As a conclusion, observation of top quark production was claimed.

Table 1 **Top quark decay modes**

Method	Observed	Background	Probability
Dileptonic	6 events	1.3 ± 0.3	$3 \cdot 10^{-3}$
Lepton + jet (SVX)	27	6.7 ± 2.1	$2 \cdot 10^{-5}$
Lepton + jet (lept)	23	15.4 ± 2.0	$6 \cdot 10^{-2}$

Figure 2



Schematic view of a typical top event with displaced secondary vertices detectable with the SVX detector. The W/W^+ decay to two jets and $e + \bar{\nu}_e$ respectively. The b quarks give rise to the detected vertices.

1.3.3 B Quarks and the SVX

As mentioned above, one of the methods of identification of lepton + jets decay is to find a b-quark tag using the SVX detector. Accurate identification of b-quarks proved crucial in the top search: it permitted to discard most background decay channels since they fortunately lacked b quarks. There are mainly two possible ways to go when looking for b. The first is search for low energy electrons or muons produced in hadronic b-decay but this is a difficult and not very reliable method. Much more performing is the vertexing method introduced at CDF by the construction of the SVX detector. The principle is the following:
As the b-quark lives for about 10^{-12} s before decaying it can fly several millimeters. When finally decaying, the created vertex will be displaced by the same distance with respect to the point of interaction. The SVX permits to identify these secondary, displaced, vertices. In principle, the SVX simply gives very precise track reconstruction of charged particles. These tracks are extrapolated back to identify the their vertex of origin. Figure 2 shows a typical top event with displaced vertices detected by the SVX. Identifying these secondary vertices is quite easy and vertexing has proven to work very well. The number of events that were identified by the SVX as containing b-quarks proved much larger than expected background making statistical fluctuations highly unlikely.
In Run II, the SVX II will play the same role in identifying b-events but, top physics will no longer be the only concern. The Tevatron produces many more b quarks than any other including specific b factories. B-physics will therefore be one of the goals of the run. So far, a problem has been that b production had hadronic background that was far to copious to allow storage of everything that looked like a b. Vertexing using the SVX II will therefore now be used for triggering decisions: the mechanisms by which it is decided whether to store an event or do discard it as uninteresting (see 2.1.3). However, vertexing is still not fast enough to treat all interactions and can be used only after that a first trigger level has reduced the number of events. This first

level must have a large rejection ratio without using vertexing. The solution is to aim mainly for the $B^0 \longrightarrow \pi^+\pi^-$ decay. By looking for a pair of opposite charge tracks with invariant mass near B^0 and placing some criteria on total momentum, it is possible to feed the second trigger level with a number of events that it can handle which is about 30,000 interactions per second. Of these, the majority does not have detached vertex and is are discarded. Study of this b-decay will hopefully give a possibility to measure CP violation.

2 SYSTEM DESCRIPTION

The silicon vertex detector SVX II is the innermost detector of the complex CDF experiment. Its main building blocks are silicon microstrip detectors and the SVX3 readout chips. This chapter gives an overview of the CDF detector and describes the SVX II and especially the SVX3 chip in some detail.

2.1 CDF

The Collider Detector at Fermilab is an assembly of several detectors formed as barrels of different sizes placed inside each other like Russian dolls.
The central part of the detector holds the tracking systems contained in a 1.4 T superconductive solenoid. These systems include the silicon inner tracker (described in detail below) nearest the beam surrounded by the Central Outer Tracker, a fast gas drift chamber. Outside of the solenoid, we find muon detectors as well as hadronic and electromagnetic calorimeters. For Run II, the COT and the inner tracking system will be new whereas calorimeters, magnets etc. will be recycled from Run I.

2.1.1 Inner Tracking Systems

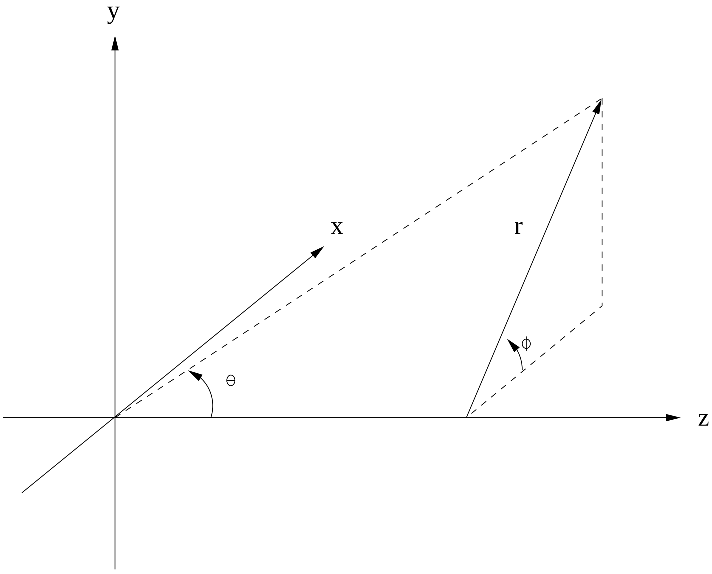
The inner tracking system consists of the silicon vertex detector (SVX II) and just outside of it, the Intermediate Silicon Layers (ISL). These detectors are supposed to give high precision track reconstruction for the region with pseudorapidity $|\eta| \leq 2^*$ to allow identification of secondary vertices for b-tagging. Both the SVX II and the ISL are built up from microstrip silicon detectors. The silicon crystals are mounted on lightweight "ladders" and are partially covered by the electrical hybrids carrying the readout electronics.
The SVX II is assembled as three cylindrical 0.32 m long barrels each containing five layers of double sided microstrip detectors. Each layer has 12 ladders making a total of 180 ladders and 405 504 electronics channels in the whole detector. The microstrip detectors measure the $r - \phi$ position of a particle with one side and the $r - z$ position with the back. By using data from several strips as described below, a precision of down to 12 μm is reached.
The ISL is built up by ladders similar but slightly longer than those of the SVX II and with the same readout electronics.
A charged particle gives rise to a signal from the silicon strips that is amplified and processed by the SVX3 readout chip as described in detail in 2.2. The chip, which has 128 channels taking data from as many strips, stores the signal on a pipeline and, when asked to, digitizes it for readout. Readout of the whole detector will take approximately 10 μs based on the expected number of hits.

2.1.2 Principle of the Silicon Strip

The bulk of a microstrip detector is made out of a wafer of n-doped crystalline silicon about 300 μm thick (depending on the layer) which is cut into 7 cm long rectangles. Narrow strips of p^+-type or n^+-type[†] silicon are formed by implanting impurities. This creates np^+ junctions that function like a diode as well as nn^+ ohmic contacts. A voltage difference is applied to the junction by connecting the bulk silicon to a positive potential relative to the p^+ strip. Apart from strengthening the diode-effect, the potential creates a field that will attract free electrons to the n^+-strips whereas holes will drift to the p^+-strips.
When a charged particle passes through the detector, electron/hole pairs are created and drift apart due to the present electric field. The accumulation of holes at the nearest strips (fig: 2) create a signal that is carried on by a metal conductor to the SVX3 chip for amplification. As the junctions might start to leak with increasing absorbed dose, a

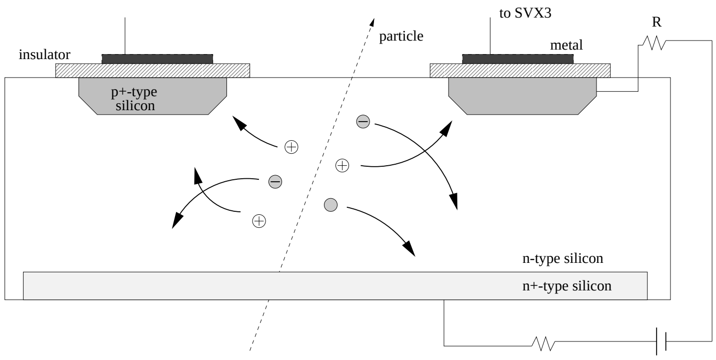
*$\eta = -\ln\tan(\theta/2)$ where θ as in fig: 1 ($\eta = 2$ corresponds to $\theta = 15°$).
†The different types of strips are used for different sides of the detector.

Figure 1



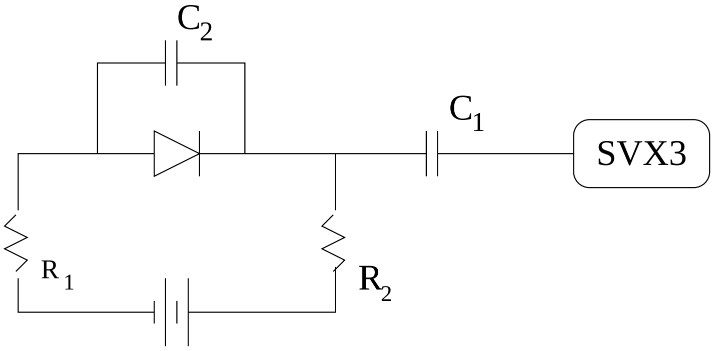
Coordinates used for the CDF detector. The beam goes along the z-axis.

Figure 2



Section of a silicon strip.

Figure 3



Circuit equivalent to a silicon strip. Capacitor C_1 represents the insulation between the strip and the metal conductor and C_2 the capacitance between strips and between strip and n^+-substrate.

layer of insulator is placed between the strips and the metal conductors connected to the chip. This way, a DC current due to leakage will not be carried on to the preamplifier which would cause the latter to saturate. During Run 1a, the SVX would have saturated with a higher dose but as the dose was low, the problem was avoided. During Run 1b, the detector had ac-coupled strips. As happened during Run I. Figure 3 shows a circuit equivalent to a silicon strip.

A single particle will create a signal in several strips which at first can appear as a disadvantage but actually permits higher precision position measurement by making a charge-weighted average of hit strips. The SVX II will use signals from three strips to determine the position of a particle that passed through.

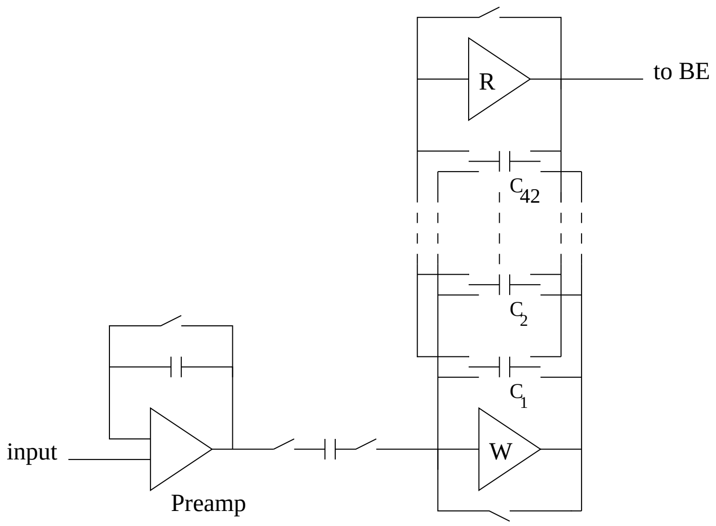
The ladders are mounted parallel with the z-axis so the strips on the junction side will be able to measure positions in the $r - \phi$ direction. To locate a hit in the $r - z$ direction, the strips on the ohmic side are at 90° or 1.2° stereo angle with respect to those on the junction side.

2.1.3 Trigger Systems

Some of the requirements on the SVX3 chip are due to the design of the CDF Run II trigger mechanisms, the decision about weather to store the information registered from a hit permanently on magnetic tape. In a modern colliding beam experiment, the frequency of events is much higher than what the information storage facilities can handle and most events must be discarded at a very early stage. In Run I, the trigger mechanisms of CDF had a rejection ratio of one saved event for each 10^5 thereby reaching an event rate of less than 10 Hz which can be handled by magnetic tape storage systems. In Run II, the luminosity will be higher and the rejection ratio must increase. However the broad spectrum of physics that is to be made with the collected data places high demand on the selection mechanisms.

With a bunch-crossing time of down to 132 ns, and at least 4 μs needed to make the first level trigger decision, all the front end electronics to be equipped with a pipeline system to buffer up to 42 beam crossings while the decision is made. Information from calorimeters, central tracking systems and muon detectors are used for the first decision whether to reject the event as uninteresting. If the event passes the test and a level 1 accept signal is returned to the front end electronics, information from the hit is fetched from the pipeline and sent on for a level 2 trigger decision. Information from the SVX II will now also contribute to the trigger decision at this point, which is a novelty for Run II. Before permanent storage, a third trigger decision is made by several parallel processors.

Figure 4



Block diagram of the SVX3 front end chip.

2.2 THE SVX3 CHIP

This section gives a description of the SVX3 chip with the purpose of making it possible to understand the testing procedures and experimental results presented in the following chapters.

2.2.1 General Description and Purpose

The SVX3 chip receives signals from the silicon microstrips as charge on any of the 128 channels. An incoming signal is amplified, stored on a pipeline and, if the right control signal comes, digitized and presented for readout. The chip consists of some 80,000 transistors of Honeywell 0.8 μm radiation hard CMOS technology. In principle the chip is divided into an analog front end (FE) part and a mainly digital back end (BE). The front end chip is responsible for amplification and holds the pipeline whereas the back end does the digitization. The prototypes used in the study were physically two chips connected together by wirebonds but in the final version, the chip will be monolithic. The new requirements on the SVX3 chip compared with the previous silicon readout chips is that it is supposed to work in a dead-time-less mode at full luminosity with beam crossings every 132 ns. That is, digitization of a registered signal from one pipeline cell must not prevent the registration of a new hit.

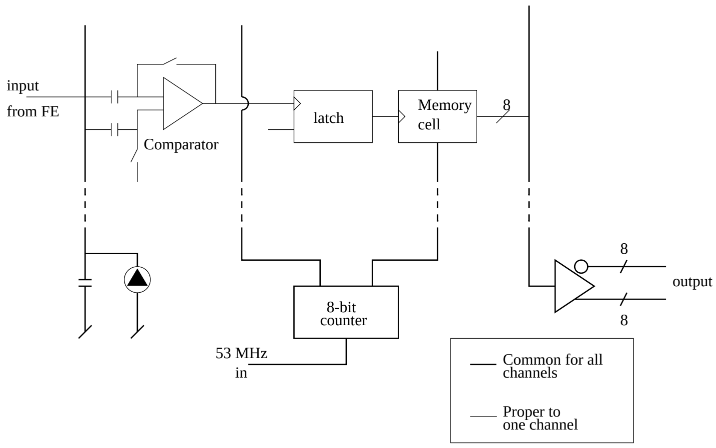
2.2.2 Detailed Description

The SVX3 is designed to work with all 128 channels in parallel and there are no differences between different channels. To follow the description, a block diagram is presented in figure 4 and 5.

In a simplified manner, a strip of the silicon detector can be compared to a small capacitor. As a particle hits the strip, a charge of corresponding to some 24,000 e is sent on to the chip. The first step in the front end of the chip is the charge-to-voltage preamplifier (PA). Reseting the amplifier requires about 1.6 μs which is far more than the normal 132 ns interval between two bunch crossings and the reset switch is activated only during the abort gaps, time intervals during which no crossings occur. This way, the signal from a single hit must be read out from the preamplifier as the difference in voltage before and after the hit.

The second step in the chain is the registration of the signal onto a cell, that is, a

Figure 5



Block diagram of the SVX3 back end chip.

capacitor of the pipeline. The pipeline capacitor is connected to the preamplifier before and after the beam crossing in order integrate the voltage difference that eventually occurs during that time. The pipeline of the SVX3 has 46 capacitors that are written to in order. The pipeline logics are designed to work with an effective pipeline depth of 42 keeping four capacitors that can be used to hold information awaiting readout once a level 1 trigger signal has been given. This permits readout from these four capacitors while the normal pipeline operation proceeds making the chip dead-time-less. The pipeline logics simply skip a capacitor marked for readout. The limited depth of the pipeline with a 132 ns beam crossing interval corresponds to a maximum delay of 5.5 μs within which a Level 1 trigger must arrive or the information will be overwritten. Pipeline logics are common to all 128 channels which therefore step through the pipeline and all read out the same cells. To allow readout of one cell while the chip writes to others, two different amplifiers (Read and Write) are used though the principle of operation is the same. There exists a 47^{th} capacitor, the reference capacitor which is used is never written to but always read out. The signal it renders, the pedestal, that is due to leakage currents or switching offsets will be subtracted from that registered by the cell before digitization.

From the pipeline, pedestal and cell voltages are carried on to the back end chip for digitization and readout. After pedestal subtraction, the voltage is fed to a Wilkinson analog-digital converter (ADC). A Gray counter starts at the same time as a voltage ramp is generated. The ramp voltage and the input voltage from pedestal subtraction are fed into a comparator. When these two voltages are equal, the comparator switches and the actual counter number is latched on to a memory cell to await readout. However, not all channels are read out depending on settings in the initialization. There are three read out modes and the chip can be set to read out:

- All channels – mainly used during chip development and testing.
- Only channels with hits, that is with a signal above a sparsification level.
- Channels with hits and neighbours – channels above the threshold and their neighbouring channels.

The latter mode will be used during Run II as it allows to calculate more accurately where the hit was using information from three channels to produce a weighted average as described earlier. The sparsification level is important for good functioning of the chip. To limit information flows out of the detector, it should be just above the pedestal

to register all hits but high enough to prevent noise fluctuations from being read out. Practically, the determination of the sparsification threshold will be a trade off between reducing noise and keeping signal efficiency.
When the digitization of all channels is finished, which takes about 2.5 μs, readout begins. Upon receiving the right control signal, the chip identifies itself and proceeds with returning data alternating channel number and recorded data for that channel. When all of the channels have been read out, a chip having finished delivering its information automatically sends a signal to the neighboring chip which initiates its own readout. Through this daisy chain, the SVX II is read out in approximately 10 μs for a normal number of hits predicted by Monte Carlo simulations.

3 RADIATION AND ELECTRONICS

3.1 FUNCTION OF MOS TRANSISTORS

The SVX3 chip consists mainly of some eighty thousand transistors of metal oxide semiconductor (MOS) technology. To understand the effects of radiation on a transistor, it is essential to have an understanding of the principles of its operation.
A normal MOS transistor has three contacts: the source, the gate and the drain (see fig: 1). MOS transistors are said to be n-type or p-type depending on the kind of minority carriers (electrons or holes) in the silicon substrate. The following description is that of a p-type MOS. Basically the transistor has the feature that the potential V_g applied to the gate controls the conductance between the drain and the source. A logical procedure is therefore to discuss what happens when V_g varies.

$V_g = 0$ In so called enhancement mode, the transistor can be said to be turned "off". The silicon works as an npn junction not allowing any notable current i_{SD} from source to drain.

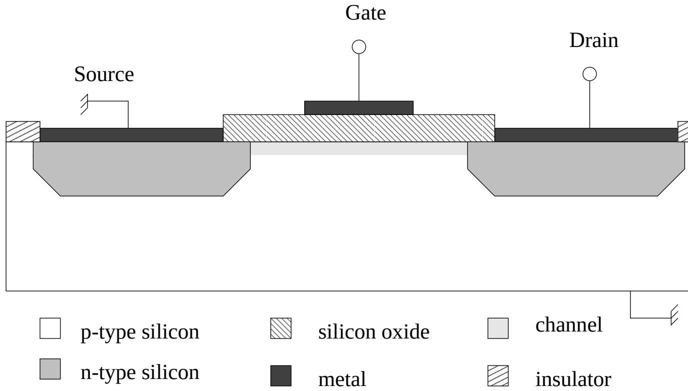
$V_g > 0$ In depletion mode, that is when a low positive voltage is applied to the gate, the created field repels holes from the area in the bulk silicon near the silicon oxide (SiO_2) called the channel.

$V_g > V_t$ As the gate voltage rises and reaches a threshold voltage V_t, the field attracts free electrons from the silicon to the channel providing the necessary carriers to allow a current i_{SD} to flow if a potential is applied to the drain. The conductance will be directly proportional to V_g for V_g between V_t and a saturation voltage V_s.

$V_g > V_{sat}$ Above the saturation voltage the concentration of electrons in the channel region becomes high enough for these electrons also to shield the bulk silicon from any additional field. The conductance will flatten out even if V_g is increased further so the thickness of the channel or the depletion depth reaches a maximum.

In practice, our chip was made out of complementary MOS (CMOS) transistors which can be described as an n-channel MOS and a p-channel MOS next to each other. Its main advantage over simple MOS transistors is that the standby power dissipation is kept at a much lower level.
The strength of the transistor is the variety of applications in which it can serve. By connecting one or a few transistors in different manners, one can easily create the most

Figure 1



Simple n-channel MOSFET.

usual components of electric circuits: resistors, capacitors etc. An integrated circuit is simply a large number of transistors connected in a certain way.

3.2 RADIATION EFFECTS

During run II, the SVX3 chips nearest the beam will be exposed to about $7 \cdot 10^{13}$ minimum ionizing particles per cm^2 over a period of two years corresponding to an absorbed dose of 2 Mrad [3]. There are mainly two types of radiation affecting electronic devices [4]: Hadronic and ionizing radiation. The SVX3 chip will be exposed to a combination of both kinds. Hadronic radiation can cause ***displacement damage*** by scattering off atomic nuclei giving rise to defects in the crystal lattice (bulk damage). In bipolar devices, these defects create notable damage but MOS devices are only affected by a slight decrease in the number of minority carriers to which they are relatively insensitive. MOS devices are thus only marginally affected by hadronic radiation. Ionizing radiation on the other hand causes atomic bonds to break by transferring energy to the electrons or creates electron/hole pairs. In both cases, free charges accumulate in the electrical insulators. To break an atomic bond, a photon must have an energy higher than the bandgap of the material (1.1 eV in silicon and 9 eV in silicon oxide). The relatively higher sensitivity of MOS technology to ionizing radiation permits us to use solely ionizing radiation to test the dose hardness of our chip. In our case, photons of energy above 1 MeV are used as discussed in chap 4.

3.2.1 MOS Transistors

Ionizing radiation on a single transistor mainly damages the insulating silicon oxide layer. This typically causes a shift in the threshold voltage, a decrease in gain and a rise in leakage currents. The mechanisms by which the transistor suffers damage are

- Trapped charge is built up in the oxide.
- Interface traps, lattice defects able to cache or release an electron/hole when stimulated, are created at the oxide/bulk silicon interface.
- Build-up of traps in the bulk silicon.

Electrons and holes are created in pairs in the silicon oxide. Often, they recombine but the electrons have a much higher effective mobility and are in greater extent carried away to the contacts by an eventual electric field leaving a net amounts of positive charge in the oxide. Thus, the net charge trapped in the oxide after exposure will usually be positive. Holes reaching the interface with the bulk silicon may capture an electron and turn into an interface trap. Chemical bonds in the oxide can act as traps when broken by the radiation. These effects are proportional to the deposited energy i.e the dose and the fraction of holes actually trapped causing charge or traps will determine the radiation hardness of the device. This fraction typically ranges from a few percent to over 0.5 for radiation soft transistors. The exact processes by which radiation hardness is obtained are industrial secrets but the basic principle is to reduce the mentioned fraction of holes that remain trapped without recombining.

3.2.2 Integrated Circuits

The effects of radiation on a single transistor have been extensively studied as mentioned above but when thousands of transistors are put together in integrated circuits, things get complicated. The effects of radiation in such circuits can vary within a large range of responses ranging from noise variations to total ceasing of function. Not only are the effects difficult to predict, they also tend to vary with time, even after the end of irradiation. A circuit not working after absorbing a certain dose can suddenly resume operation after a while only to again cease to work somewhat later. The formidable number of variables that will affect the dose response of a certain circuit make it difficult to accurately predict or simulate the effects with computer programs as for example Spice. Testing of the circuit under conditions as similar as possible to those of the circuits operation becomes unavoidable for realistic simulation of the radiation damage.

4 DOSIMETRY

As described in chapter 3, the damaging effects of radiation on MOS devices are mainly due to ionization. To simulate the ionizing radiation of the Tevatron, we used gamma rays from an old Co^{60} source normally used for irradiation of unfortunate mice at the Life Science department. Energetic photons can well enough simulate the ionizing effect of the mix of particles and photons that will be present during Run II. Gamma rays also have the advantage of not leaving the irradiated material active once irradiated.

4.1 SETUP

4.1.1 The Co^{60} Source

The active cobalt lies hidden in a 1.5 m high concrete cylinder with a diameter of 0.7 m. When an irradiation is to start, the cobalt is lifted to a spot right in front of an opening in the cylinder through which the gamma rays pass. A metal fixture was made to hold steady the board on which the chip is mounted. The cobalt has a physical size of a few cm^3 and will not quite behave as a point source as discussed later. During irradiation, a significant part of the room is exposed to direct radiation. A thick concrete wall divides the room and forms a corridor to the exit. This corridor is out of range for both direct and once-scattered radiation and the computer used in the experiment is placed there along with some power supplies. Two dosimeters attached on the computer during an irradiation registered 0.0025 rad/h giving a mere 0.04 rad for each Mrad the chip is exposed to. To operate the source, there is a control panel outside of the room.

4.1.2 The Board

The chip is attached to a printed circuit board mounted on a metal fixture holding it in position during irradiation. The board is placed with the chip on the far side of the source so that the gamma rays have to penetrate it before reaching the chip. Also, for reasons described in 4.5.4, a 1 mm thick piece of aluminium is glued between the chip and the board. The board is made of several layers adding up to: 0.5 μm Au, 100 μm Cu and 1.175 mm FR4 (a plastic material). The active circuit is formed on the far side of the chip from the source adding an extra 375 μm of silicon for the rays to go through.

4.2 BASIC CONCEPTS

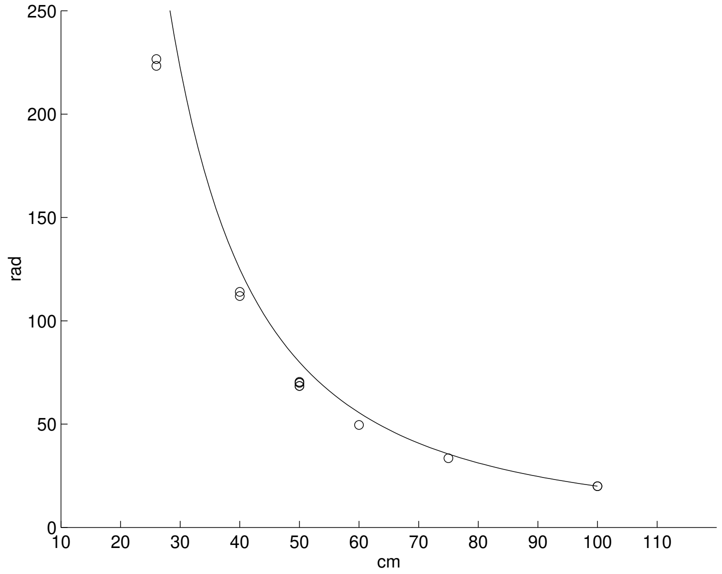
As we will be using some dosimetry concepts below, it can be useful to define them properly.

Absorbed dose (also called dose or total dose) is the mean energy absorbed per unit mass of exposed material at a certain point. The SI unit of dose is the gray defined as 1 Gy = 100 J/kg but one commonly uses the rad: 1 rad = 1/100 Gy = 100 ergs/g. The often encountered unit rem measures the dose absorbed by human tissue taking into account properties of different types of radiation. For gamma rays 1 rad = 1 rem.

Dose rate is the rate of change of the absorbed dose with time usually measured in rad/s. If dD is the change of dose during a time interval dt, the dose rate will be dD/dt. In our case, the dose rate will be almost constant during exposure but in the case of pulse irradiations, the term dose rate usually is used for the maximum dose rate.

The theoretical definition of the dose usually cannot be used for dosimetry as the region of interest (the inside of transistors) is inaccessible. Instead, it is necessary to first measure the energy deposited in some reference material (typically a dosimeter) and then relate it to the absorbed dose in the material and region of interest.

Figure 1



Absorbed dose vs. distance from the source. The solid curve is that of an ideal point source giving the same dose at 1 *m.*

4.3 INTENSITY

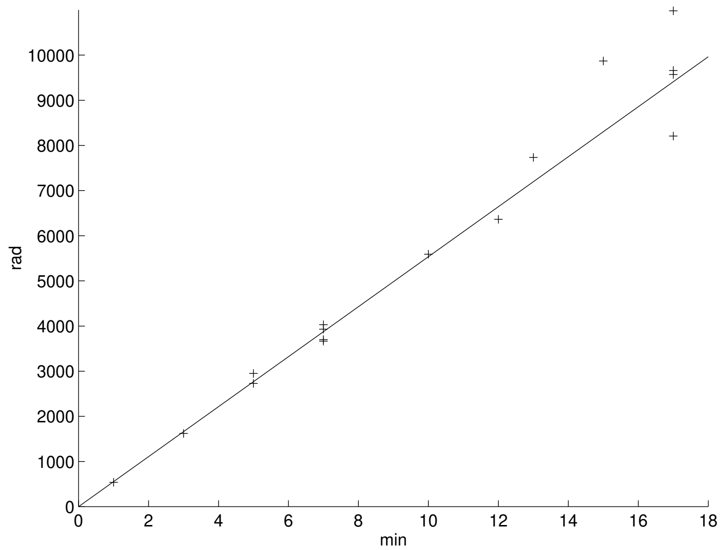
A first series of measurements was made to get a rough idea of the source's intensity. A simple direct-readout dosimeter was positioned at different distances from the source and exposed for one minute. As seen in figure 1, the measured doses do not quite follow the theoretical curve of an ideal point source giving the same dose at 1 m. This is expected due to the non point-like geometry of the source.
We aimed at irradiating the chips to a minimum of 2 Mrad and for practical reasons, the irradiation had to be done over a maximum of two days. To achieve a dose rate high enough to allow this, we had to reduce the distance between source and chip to about 15 cm. At such a distance, the uncertainty in dose caused by small uncertainties in distance would be considerable. To keep the chip at exactly the same position during every single exposure, an aluminium fixture was constructed. When attached to the fixture, the chip was held at 14 ± 0.2 cm.
A second series of measurements was now made by exposing thermo-luminescent dosimeters (TLD) placed at the chip position for different amounts of time (fig: 2). The least square fit of the dose (slope of line in figure) is 554 rad/min with an RMS error of 51 rad/min or 9%.
The uncertainty due to position variation can be estimated. Let l be the distance from the source to the object and l_f the distance set by the fixture. The dose rate at as function of l then becomes

$$D(l) = 554 \left(\frac{l_f}{l}\right)^2 \tag{4.1}$$

The change in rose rate for a small shift in l is then

$$\begin{aligned} \left(\frac{\partial D}{\partial l}\right)_{l=l_f} &= -2\left(\frac{554}{l_f}\right) \\ &= -79 \quad \left[\frac{\text{rad}}{\text{cm}}\right] \end{aligned} \tag{4.2}$$

Figure 2



Absorbed dose as function of time at chip position of the chip. The straight line gives the least squares fit to the data and has a slope of 554 *rad/min.*

In our case, the uncertainty of 2 mm becomes 16 rad/min or 3%. Some TLDs were exposed at positions close to that of the chip to test agreement with equation 4.1. The results (fig: 3) show a fair agreement considering that the effect of not having an ideal point-source will be important at such close range.

4.4 PHOTON SPECTRUM

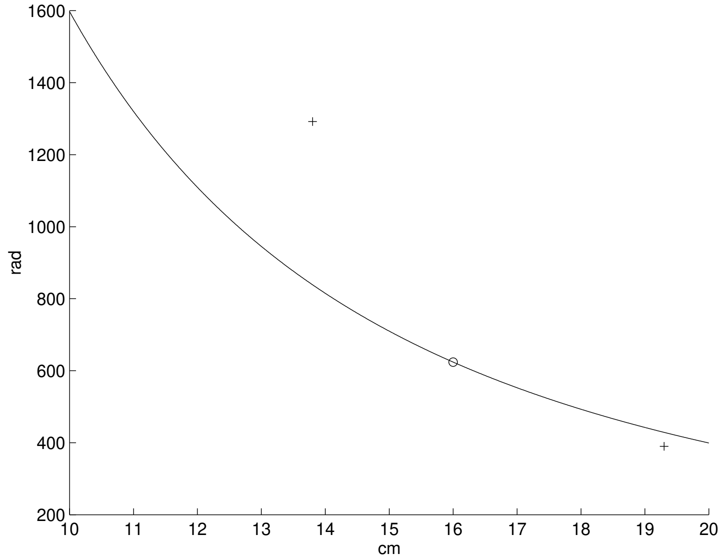
Active Co^{60} produces gamma radiation in a three step process. A primary reaction makes the Co^{60} β decay to Ni^{60} which immediately decays itself through two successive transitions to its ground state emitting two photons of 1.17 MeV and 1.33 MeV respectively. Unfortunately, the actual spectrum of photons will not only contain the two above mentioned wavelengths. Compton scattering inside the cobalt and in the walls of the cavity surrounding it generates photons of lower energy. Their energy according to the Compton formula (4.12) should range up to 0.2 MeV. However, experimental results [4] show a spectrum which includes energies up to about 0.5 MeV with a peak around 0.25 MeV. If they constitute an important part of the total gamma rays, the low energy photons can impact dosimetry considerations. Calculating their abundance is therefore important.

For a fixed exposure time, the integrated energy of the photons of a beam (hereafter called beam energy) penetrating some material decreases with an exponential factor as

$$E_{out} = E_{in} e^{-(\mu_{en}/\rho)\rho x} \tag{4.3}$$

where x is the thickness of the material, ρ its density and ρx is defined as the ***mass thickness***. The mass energy absorption coefficient μ_{en}/ρ is dependent of the material considered and of the photon energy. The similar more familiar equation relating the intensity of a beam differs in that it uses the mass attenuation coefficient μ/ρ. We define the coefficient q as the attenuation factor for a certain obstacle in the way of our beam. Let's make the somewhat simplifying assumption that we have photons of only two energies 0.2 MeV and 1.25 MeV. We call E_l and E_h the total energy of the 0.2 MeV and 1.25 MeV photon beams respectively and the doses these two rays deposit in our dosimeters are denoted D_l and D_h. The dose we measure is then simply D_t where

Figure 3



Dose at different distances (+) around the fitted dose at the chip position (○). The full line indicates a theoretical curve passing through ○.

$D_t = D_l + D_h$.
We measured $D_t = 90$ rad/min at 50 cm from the source for a 78 s exposure. The same measurement was repeated with different metal plates as shields between the source and the dosimeters. The shields used were: 6.35 mm aluminium, 6.3 mm lead and a thinner sheet of 0.8 mm lead. For each of the energy components of the beam, the attenuation factor will be different but known since we know the thickness and μ_{en}/ρ for each metal. We now assume that for a given photon energy, the dose deposited is proportional to the beam energy, $D_i = \alpha_i E_i$ where $i = l, h$. Thus for attenuated beams, we have

$$\begin{aligned} D'_t &= \alpha_l q_l E_l + \alpha_h q_h E_h \\ &= q_l D_l + q_h D_h \end{aligned} \tag{4.4}$$

We measure D'_t and know the factors q_l and q_h. To solve for D_l and D_h, we now need at least two measurements with different attenuation coefficients. The measurement was repeated for three different shieldings, yielding an over-determined system of linear equations.

$$\begin{pmatrix} 84.6 \\ 63.5 \\ 84.5 \end{pmatrix} = \begin{pmatrix} 0.9540 & 0.9570 \\ 0.0145 & 0.8063 \\ 0.5908 & 0.9736 \end{pmatrix} \begin{pmatrix} D_l \\ D_h \end{pmatrix} \tag{4.5}$$

The left matrix holds the measured doses for the aluminium, the thick lead and the thin lead shields respectively. The second matrix contains the attenuation coefficients for each shield and wavelength. Least squares fit now gives

$$\begin{pmatrix} D_l \\ D_h \end{pmatrix} = \begin{pmatrix} 9.91 \pm 1.55 \\ 79.38 \pm 7.94 \end{pmatrix} \tag{4.6}$$

Where the given "uncertainties" in D_l and D_h should be interpreted as the change in the parameter in question giving a one unit change of the χ^2 while the other parameter is kept constant. As a second check, we see that $D_l + D_h = 89.30$ which is close to

Table 4 **Mass energy absorption coefficients for TLDs and Silicon**

Γ Energy (MeV)	μ_{en}/ρ Si (cm^2/g)	μ_{en}/ρ TLD (cm^2/g)	Λ
0.20	$2.905 \cdot 10^{-2}$	$2.942 \cdot 10^{-2}$	0.987
1.25	$2.652 \cdot 10^{-2}$	$2.938 \cdot 10^{-2}$	0.903

the independently measured $D_t = 90$. We can now deduce that the proportion of the deposited dose that is due to the 0.2 MeV photons is

$$\frac{D_l}{D_l + D_h} = 11\% \tag{4.7}$$

4.5 COMPLICATING FACTORS

The cross section of photons is not the same for every material and different materials will therefore absorb different amounts of energy from the same radiation. The dosimeters used in this study are not made out of silicon and so, the dose measured will differ from that absorbed by the silicon. A calculation of the relation between these two doses is therefore crucial.

4.5.1 Charged Particle Equilibrium

When photons are sent through material, they deposit energy producing energetic electrons which themselves travel in the material depositing their excess energy. When the beam enters the material, the density of scattered electrons increases initially but stabilizes after a certain distance. At this stage, a small volume receives on average as many electrons from neighboring material as there are electrons leaving it. One defines [4] ***charged particle equilibrium*** (CPE) as the state in which the energy carried in to a volume by electrons equals that carried away by electrons. The key word here is "by electrons". The thickness of material required for CPE to establish is called ***equilibrium thickness***. The calculation of this thickness is complicated but a rule of thumb is that it is no longer than the distance traveled by the most energetic scattered electron.
In the parts of the irradiated object where CPE is established, the ***equilibrium absorbed dose*** will be

$$D_{eq} = \phi_\gamma(\mu_{en}/\rho) \tag{4.8}$$

Where ϕ_γ is the photon energy fluence and μ_{en}/ρ is the ***mass energy absorption coefficient***. Were CPE not established, the absorbed dose would not be a function of the photon fluence alone. In the case of our experimental setup, ϕ_γ will be the same for the chip and the TLDs when they are at the position imposed by the fixture. We have

$$\Lambda \equiv \frac{D_{eq}^{TLD}}{D_{eq}^{chip}} = \frac{(\mu_{en}/\rho)_{TLD}}{(\mu_{en}/\rho)_{chip}} \tag{4.9}$$

As the mass energy absorption coefficients are material constants for a given photon energy, equation (4.9) gives us the relationship that we sought between dose absorbed by the dosimeter and that absorbed by the silicon.
The TLDs used for calibration of the source are made of lithium borate crushed powder ($Li_2B_4O_7$:Cu) which has a Z value matching that of human tissue (7.6). Lacking data about its mass energy absorption coefficient, we use that of tissue
Table 4 shows that the factor Λ is larger for low energy photons and so the low energy component of the radiation has relatively larger impact on the dose in silicon than the high energy component. Adjusting for this effect, equation (4.7) becomes:

$$\frac{\Lambda_l D_l}{\Lambda_l D_l + \Lambda_h D_h} = 12\% \tag{4.10}$$

However, the interesting figure in our case is the coefficient we can call λ relating the dose measured by the TLDs and that received by the silicon, which will be a linear combination of Λ_l and Λ_h weighted with the relative abundance of the corresponding gamma energy.

$$\begin{aligned} \lambda &= \frac{D_{Si}}{D_{TLD}} = \frac{\Lambda_l D_l}{D_l + D_h} + \frac{\Lambda_h D_h}{D_l + D_h} \\ &= 0.912 \end{aligned} \tag{4.11}$$

We measured a dose rate of 554 ± 51 rad/min which becomes 505 ± 49 rad(Si)/min when multiplied by λ. In the following text, all doses will be given in rad(Si) taking this factor into account.
Some literature [4] suggests using a filter consisting of a shield with 0.7 mm lead and 1.5 mm aluminium to filter out the low energy rays. If we use equation (4.3) and simply add up the mass thicknesses* weighted with the thickness of the material in question, we can calculate the attenuation of shields with several layers. The 0.2 MeV rays are attenuated by a factor 0.4 but the intensity of 1.25 MeV photons is also reduced by 6%. However, the precision of the dose measurements are not such that this loss of intensity is motivated by the slight gain in accuracy it would imply for some measurements. We conclude that it would not be to our advantage to take any measures to filter out low energy photons.

4.5.2 Achieving CPE

To be able to use equation (4.9) we must find out weather CPE is established in the chip or not. As mentioned above, CPE is established after a certain depth into the penetrated material, the equilibrium thickness. The chip only contains 375 μm of silicon. Will this be enough? The equilibrium thickness is roughly equal to the range of the electrons knocked loose by the photons through Compton scattering. To estimate the equilibrium thickness, we need to estimate this range.

4.5.3 Electron range

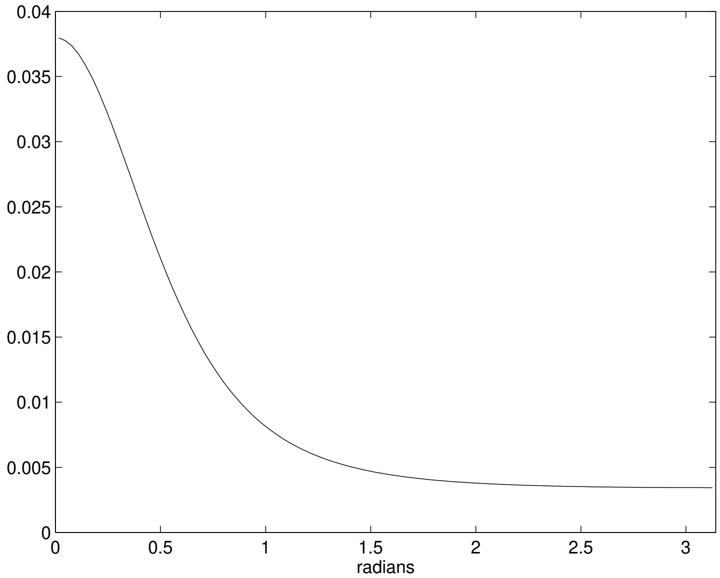
Consider the collision between a photon with energy E and an electron. After the collision, the photon has energy E' and is scattered at angle θ. The classical Compton formula gives

$$\frac{1}{E'} - \frac{1}{E} = \frac{1}{m_e c^2}(1 - \cos\theta) \tag{4.12}$$

The energy $E - E'$ is transfered to the electron and for 1.25 MeV photons, the maximal energy that can be transfered is 9.98 MeV which occurs in the case of direct back scattering. In silicon, such an electron will travel [6] about 2 mm. We have only 0.4 mm of silicon. CPE apparently will not be established. However, if the electrons with these energies make out only a small fraction of all electrons, we might be close to having CPE. To investigate this, we need to calculate the electron energy spectrum and energy distribution of the electrons.
Since the energy of the electron is closely linked to the scattering angle of the photon, we need their angular distribution. The Klein-Nishina formula gives the differential scattering cross section:

*This is a simplification but for photon energies below 20 MeV simple additivity can be used with small errors [5].

Figure 5



Fraction of photons scattered at 1.2 *MeV within* $[\theta; \theta + d\theta]$ *for* $d\theta = \pi/100$ *as function of* θ*.*

$$\frac{d\sigma}{d\Omega} = Zr_e^2 \left(\frac{1 + \cos^2\theta}{2(1 + \alpha(1 - \cos\theta))^2} \right) \left(1 + \frac{\alpha^2(1 - \cos\theta)^2}{(1 + \cos^2\theta)[1 + \alpha(1 - \cos\theta)]} \right) \tag{4.13}$$

Where Z is the atom number (14 for silicon), r_e is the classical electron radius and $\alpha \equiv h\nu/m_o c^2$. We are interested in the distribution of gamma rays as function only of θ which can be obtained by integrating the cross section $d\sigma/d\Omega$ with respect to φ. In this case, as there is no φ dependence, we simply get a factor of 2π. The distribution is shown in figure 5.
The Compton formula (4.12) also gives us at hand the energy transfered to the electron for any θ shown in figure 6.
Combining this information plotting the electron energy verses the angular distribution matching the respective θ gives the energy spectrum of the electrons that we sought (see figure 7).
As we are mainly interested in knowing the role of electrons with high energy that disrupt the CPE, the most interesting information is the fraction $\eta(E)$ of electrons with energy higher E. As we know the fraction $h(\theta)$ of electrons with energy $[E(\theta); E(\theta) + dE]$, we calculate:

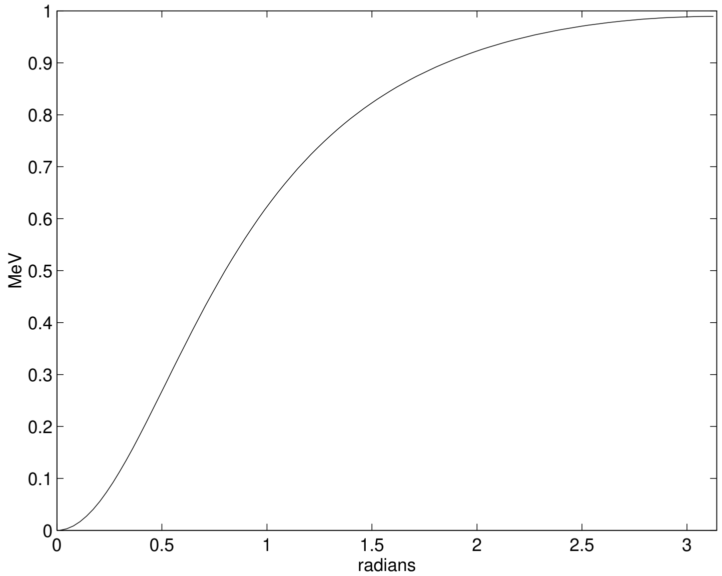
$$\eta(\theta) = \frac{\int_0^\theta h(\varphi)\, d\varphi}{\int_0^\pi h(\varphi)\, d\varphi} \tag{4.14}$$

Plotting $\eta(\theta)$ against matching $E(\theta)$ now renders figure 8. It becomes apparent that the electrons reaching further than one millimeter will be only a small fraction of all electrons.
Figure 8 shows that about 70% of the electrons have energies below 0.7 MeV and [6] thereby ranges of about 1 mm which can therefore be thought of as an approximate equilibrium thickness.

4.5.4 Interface Dose Enhancement

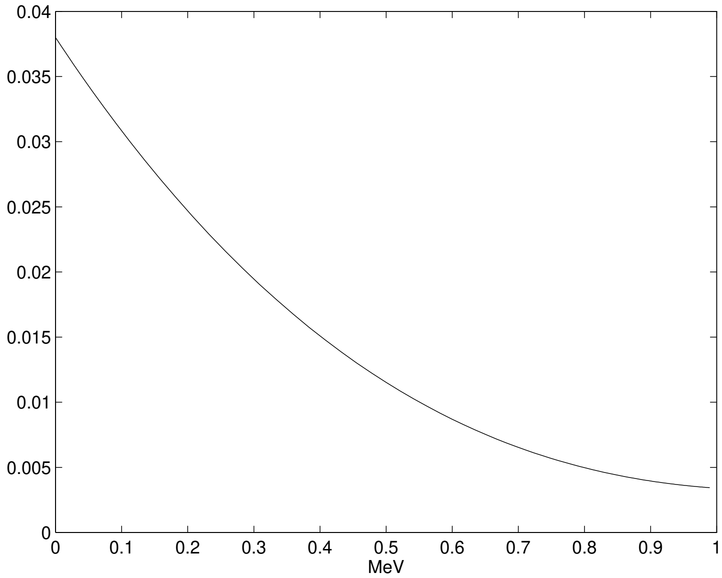
At the interface between two materials, the absorbed dose should be discontinuous according to equation (4.8). In reality, non equilibrium electron transport across the

Figure 6



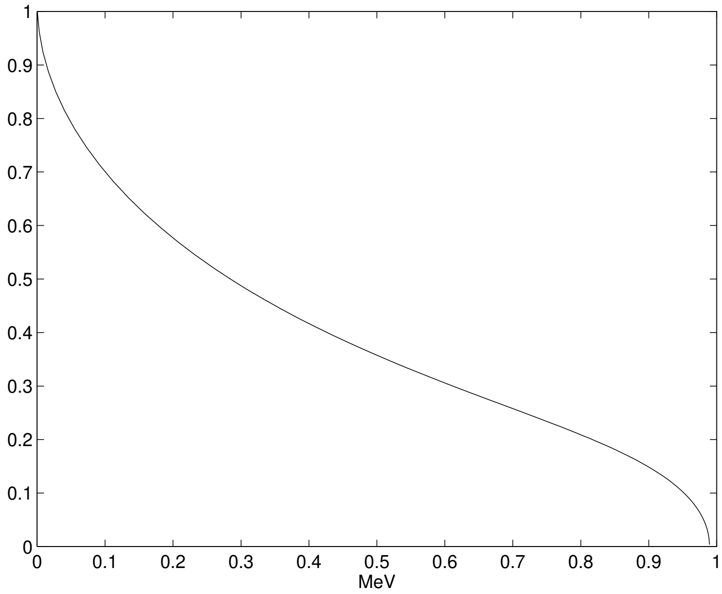
Energy transfered to the electron by Compton scattering of a 1.2 *MeV photon as function of the photon scattering angle* θ*.*

Figure 7



Fraction of electrons with energy $[E; E + dE]$ *as function of* E*.*

Figure 8



Fraction of scattered electrons with energy > E verses E.

interface results in fluctuations of the absorbed dose for several equilibrium thicknesses on each side of the interface. The dose can be both enhanced and reduced by up to 20% at a gold–silicon interface. In our case, there are several interfaces and the silicon of the chip may not be thick enough for these effects to be attenuated. In order to reduce interface enhancements, 1 mm of aluminium was placed under the chip. Aluminium has a mass energy absorption coefficient close to that of silicon thereby making the transition softer and potential enhancements weaker. Still, there should ideally have been a substantially thicker layer to totally avoid the problem. Interface dose enhancement therefore remains a source of uncertainty as to the determination of dose. The aluminium layer also assures that we will be close to a state of CPE as discussed above in section (4.5.2).

4.5.5 Dose rate

In our case as in many other studies, one wants to investigate in a brief period of time the effects of low dose rate radiation that the object will be exposed to over several years. This is done by exposure to radiation with dose rates many orders of magnitude higher. Are the effects of these two forms of radiation the same? Radiation damage usually is not static nor non-reversible. For years after irradiation, the damages can increase or anneal. Historically, the changes of radiation effects after exposure are called annealing even if damage increases. At a very low dose rate, the annealing process goes on simultaneously as the radiation affects the object. At high dose rates, there is simply no time for any appreciable annealing to take place. To attain the same effect there is the option of speeding up the process by raising the temperature as annealing shows a strong temperature dependence. The remaining question is if high dose rate irradiation with subsequent appropriate high temperature annealing is equivalent to low dose rate exposure.

Extensive documentation [7] points towards there being a notable dose rate dependence for bipolar devices. However, the situation is different for MOS technology [7] for which high temperature annealing is a good substitute for time. A week at 100°C is equivalent to several years at room temperature but our experiments showed that a single day at 100°C brought about almost the same effect. According to the studies cited above, the effects on devices exposed at low dose rate turned out to be somewhere in-between those observed before and after annealing of devices irradiated at high rate. To be on the safe side when studying the radiation hardness, the recommendation therefore is to perform the planed tests both before and after annealing.

4.5.6 Temperature

Due to the high number of possible responses and failure modes, it is difficult to predict the impact on radiation damage that temperature during irradiation could have. More detailed studies have been made for military use but are not available in open literature. A test of DRAM devices [8] from different manufacturers showed little or no temperature dependence for the range $-50°$C to $20°$C. When operated in the Tevatron, the electronics of the SVX II maintained at $10°$C by a cooling system. During the irradiations of the test boards, no cooling system was available but the chips did not get notably warmer than room temperature.

4.5.7 Powering

The powering and operation of a circuit during irradiation is an important factor for realistic radiation damage testing. On the single transistor level, the presence of a bias voltage will obviously have impact on charge transport and can also affect trapping mechanisms. It is known since the early studies of radiation effects on MOS devices [4] that applied bias voltage has a major impact on the responses. Sign and amplitude of the gate voltage affect the threshold voltage. Operation frequency and source/drain biases also have to be taken into account for the prediction of the exact total dose responses of a transistor [4]. Attempting to predict the way in which operation will alter the radiation responses is therefore a formidable task. The easy solution is to power and operate the chip in a similar way as during its use later.

4.6 CONCLUSION

We do not know to what extent CPE was established in the chip during irradiation. However, the gluing of 1 mm of aluminium between the chip and the board most certainly brought us close to CPE and lowered the effects of interface dose enhancement. To simulate the low dose rate (about 2 rad/min) that the chip will experience during Run II, we exposed the chips to radiation at a dose rate of 505 rad(Si)/min and, once the planed total dose was reached, the chips were let to anneal the effects for a week at $100°$C.

5 CHIP TESTING

5.1 TEST CONDITIONS

Irradiations were made using the cobalt source extensively described in chapter 4. As light can induce charge in silicon, we covered the chip with a black cloth during irradiation and by a metal lid during testing in the lab. We mentioned earlier (4.5.7) that electric fields are an integral part of the radiation damage mechanisms and that operation therefore is crucial for obtaining realistic simulations. The chip was not connected to any silicon strips but to simulate the load of these, some channels were connected to capacitors of either 10 or 22 pF corresponding roughly to the load of the different strips (straight or at stereo angle). A personal computer was operating the chip at 50 MHz (close to the 53 MHz used during Run II) through the locally constructed "PATT" chip test setup [9] described below (5.1.1). Testing of the chip was done partially in-between irradiations in the lab but mainly on-line during exposure as the operation of the chip allowed to collect data continuously. Typically, the chip was left exposed overnight thereby receiving about 0.4 – 0.5 Mrad.

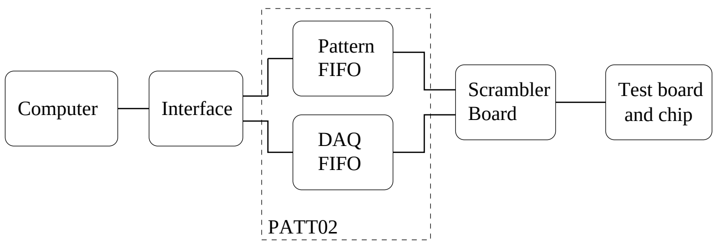
During the study, three chips were irradiated and tested. The chips/boards were named H3, H6 and H7 in the order of assembly. Logs of the exposures can be found in appendix B. In a first series of two irradiations, H3 was brought up to 0.9 Mrad, let to anneal for one day at 100°C and irradiated again bringing it up to 1.6 Mrad. After that, the chip was left to anneal the effects for a week. The second board, H6 exposed to 1.9 Mrad over a weekend in order to rapidly produce two boards with doses corresponding to Run II. Later, H3 was exposed reaching a total of 3.5 Mrad and H6 was irradiated in two steps reaching 5.8 Mrad in an unsuccessful attempt to see when the chip would stop working. The testing procedures were modified during the irradiation of H3 and H6 as the first results were used to ameliorate the routines. Also, the handling of the boards, especially concerning time gaps between irradiations and between exposure and testing was anything but systematic. A third chip, H7, was therefore assembled and irradiated to 2 Mrad in a more careful and systematic manner. After a week of annealing, it was exposed further reaching a total dose of 3 Mrad.

5.1.1 The PATT System

For the SVX3 chip to operate, patterns of control signals must be provided and a data acquisition system is necessary. When used in the SVX II detector, a specially built system will operate the whole detector (see [10]). For the development and testing of the chip, this system would have been unpractical and a smaller system was developed [9] to make it possible to use a normal computer (PC or a workstation) for both pattern generation and data acquisition. A brief description of the system is presented here.

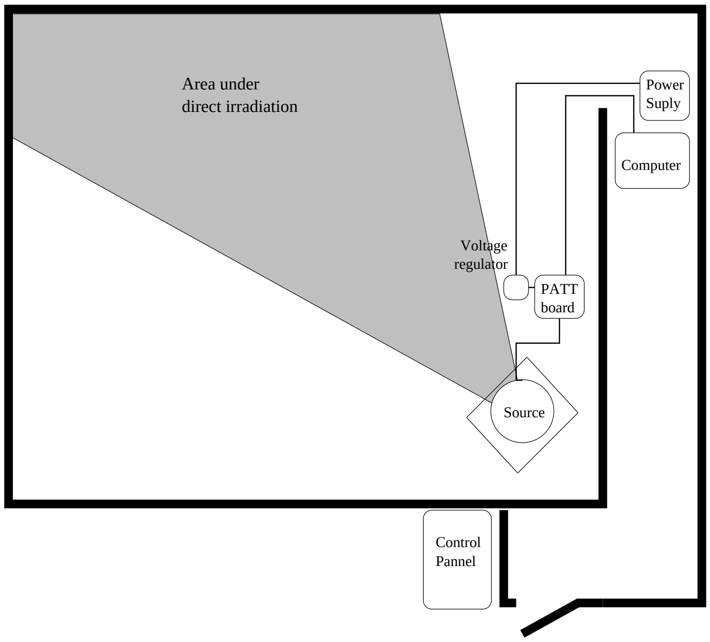
To satisfy the demand for flexibility and rapid switching between patterns, a computer was used rather than a pattern generator. The disadvantage of a computer is that its output is relatively slow (less than a MHz) compared with the 50 MHz required.

Figure 1



Schematic diagram of the PATT system setup for chip testing.

Figure 2



The room containing the cobalt source which is normally used by the Life Science division for irradiation of mice.

Receiving data from the chip would at that speed would also be difficult and the timing between successive output bits can vary significantly. The PATT system solves these problems. The pattern generated by the computer is sent to the PATT02 board (fig: 1) through an interface which will be different depending on the computer used in each case. On the PATT02 board, the incoming pattern is stored in a 16 K FIFO memory (the "pattern FIFO") which then delivers the signals with desired frequency (determined by a clock oscillator on the PATT02 board) and proper timing. This does not permit a continuous operation of the chip but instead short bursts of operation which however is fully sufficient for the testing. From the pattern FIFO, the data is clocked on to the scrambler board which acts as an interface between the chip and the FIFOs. This board generates the differential signals that are sent to the chip and carries the necessary drivers and receivers. Data coming back from the chip passes the scrambler and is sent on to a data acquisition FIFO (DAQ FIFO) where it is stored until the entire pattern is finished. Only then is the data passed on to the computer input.
The PATT system includes not only hardware but also a procedure library that can then be used in a master program. The latter is not provided an must be written for each application which may be seen as a disadvantage but gives the system a high level of flexibility to test the chip in different and maybe unanticipated ways. The main structure of any such program is to create a pattern that is to be run, send it to the chip with the adequate initialization data, collect the returning data and treat it.

5.1.2 Setup

To protect it from irradiation, the computer was safely placed behind a protective wall (fig: 2) during exposure of the chip. Two 6 m long cables connected it to the PATT board which was next to the source but protected by lead bricks. Two power supplies were also placed behind the wall and voltage regulators next to the PATT board assured that the tensions were not affected by the length of the cables. A shorter 60 cm cable connected the PATT board to the smaller board on which the chip was mounted.

5.2 TESTS

The purpose of the testing was to check operation of the chip during and after irradiation up to at least the 2 Mrad expected during Run II. Eventually observed damages were to be studied and hopefully understood. The tests therefore concentrated on general functionality control of the irradiated chips and on monitoring different characteristics. Those affecting the signal to noise performance were of special interest. As described previously, tests were performed on-line by the PC in highest possible extent as this permitted us to collect more data points but some tests had to be done in the lab manually in-between irradiations.

5.2.1 In-lab Test

DC Voltages and Currents

Certain currents and voltages in the chip can be measured and controlled mainly to be able to adapt and optimize operating points for minimal power consumption. Higher quiescent currents can for example lower the noise but also raise power consumption. When back in the lab after irradiations, a selection of DC voltages and currents were measured while a work station operated the chip with a program running a pattern that keeps the front end preamplifier in a reset mode and the back end in digitize mode. Constantly resetting the preamplifier is necessary so that it does not charge up which would affect the measurements of the input voltage (described below). Digitize mode has the advantage of keeping the back end idle while no control signals are given. The measured voltages and currents are then:

Voltages:

- FE PA input The front end preamplifier reset voltage provides a direct measure of the threshold voltage of the input transistor. It is one of few possibilities to monitor the variation of threshold voltage of a transistor enabling us to compare it with the data [11] obtained from the chip manufacturer Honeywell.
- FE Iset 1 Sets the current through the input transistor of the front end chip fixing its operating point.
- FE Iset 2: Current setting the DC level of operation in the pipeline amplifier.
- BE Iquiescent: Sets the general operating point for the back end chip.
- BE Ramp rate: Sets the rate of the voltage ramp in the back end ADC.
- BE I drivers: Sets the tension for the output voltage drivers.

Currents:

- AVDD 2 Power supply for the input transistor of the front end chip.
- AVDD *(total)*: Power supply for the remaining transistors of the front end chip.
- BE DVDD: Power supply for the logics of the back end chip.

The front end preamp input and back end ramp rate voltages are the only ones of these for which shifts would have simple interpretations but drastic changes of other voltages would raise a warning flag that further investigation was necessary. The same can be said about the currents but a sharp rise in current consumption would affect the power dissipation of the whole chip and require the adjustment of the planned cooling system.

Propagation Delays

When data is read out from the chip, it is delivered over 8 different bits. When all bits have acquired their correct state (high/low) for sending a word, this is signaled by the switching of a 9^{th} data valid bit. All bits, including data valid follow the back end clock with some small delay. The delay between the edge of the data valid bit and that of the data bit is crucial. The readout board can be set to readout expecting different delays and can therefore handle a certain dose dependence for the propagation delays. However, if the delay between different combinations of edges (rising/falling) for the data valid and the different bits show different response to radiation, it could become impossible to find a board setting for which all bits can be read out. To measure this, the propagation delays were measured between:

- Rising/falling edge BE clock and rising/falling edge of data valid respectively.
- Falling edge of BE clock and falling/rising edge of bus 0.
- Rising edge of BE clock and falling/rising edge of bus 0.

Pipeline Delay

The architecture of the SVX3 chip is such that it continuously acquires analog data samples with a 132 ns sampling rate. Any sample can be selected for digitization and readout after it has been acquired. The selection is made by an external trigger called level 1 accept. This happens a few μs after the corresponding event occurred. Since the event, new data might have been acquired and the chip must retrieve the data from the pipeline. The the number of pipeline cells the chip is supposed to go back to fetch the relevant data can be set to any value between 1 and 45 during the initialization of the chip. To test this system, a program was written that ran a pattern 42 times for each of the possible pipeline delay settings. In each of these iterations, the l1a trigger signal was given at different FE clocks (for each of which the pipeline counter advances) and the program checked if the cell read out corresponded to the actual delay setting and trigger position.

Gain

The gain of the chip is determined by a combination of two different factors:

- The preamplifier gain which, as long as the preamplifier open loop gain remains high is given by a ratio of capacitors.
- The ADC converter is based upon a voltage ramp which is controlled the ramp rate voltage. The source of this voltage is the diode of a current mirror and goes to an external resistor used for setting the ramp current.

As any dose response from the gain would have an clear impact on measured pedestal, it was important to measure it. A program sent a charge injection and readout pattern to the chip 10 times, each time varying the level of injected charge. Comparing injected charge and measured output from the chip gives a direct measure of the gain in ADC counts per charge.

5.2.2 On-Line Tests

The operation and on-line testing of the chip during irradiation was implemented with a personal computer running a program written by Igor Volobouev. The program keeps the chip in operation and with a preset period (typically 30 – 90 min) runs a series of tests described below and stores the data. The sequence of operation is:

1. In between two measurement cycles, a dummy program is run which injects charge in some channels and then reads out the chip each time using a different cell. It is built up as:
   - A pattern with main blocks: initialization, acquisition, digitization and readout which takes 80 μs.
   - During the remaining of a millisecond, the chip is powered, but with all control signals fixed.
2. Tests are performed for about 8 minutes.

During a test cycle, the following measurements are made.

Rise time

The integration time for the preamplifier will be set to the longest time allowed by the beam crossing time. The rise time of the preamplifier must then be adjusted for optimal signal to noise performance. A too short rise time allows high frequency noise to pass through whereas a too short rise time might cut of the signal before it has reached full amplitude. In the SVX3, an initialization variable in the range 1 – 7 controls the rise time (decreases with rising variable value). The rise time is not expected to vary much with variation. When operated in Run II, the bunch crossing time will put an upper limit on the possible integration time. As this time may vary during the run, the possibility of adapting the bandwidth setting was necessary.

Ramp Pedestal

When the amplified voltage from a signal is to be converted to a digital number of counts, the ADC uses a voltage ramp rising while a counter keeps track of time. The slope is fixed but a initialization variable allows to control the offset or ramp pedestal. As the ADC counter only has 8 bits, a maximum of 255 counts is possible. One wishes range of counts to be such that noise shows (at an average level of about 10-20 counts) as well as the strongest signals. To attain this, the ramp pedestal can be set to a value between 3 and 15. The step with which the pedestal increases with setting varies and is relatively large for setting 3 – 5 and 12 – 15. The on-line program tests the ramp pedestal by reading out the value of selected channels at for each setting after injecting a constant charge. The plot of counts vs. setting normally has the general apparence of figure 3.

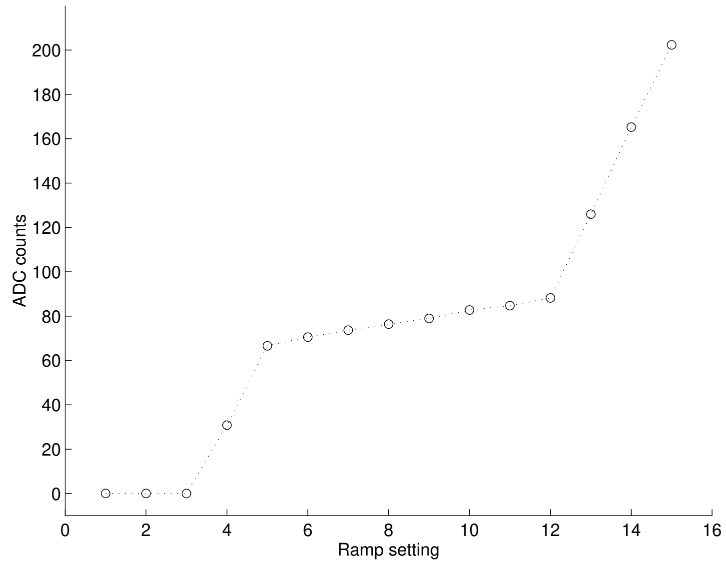
Noise

To measure the noise, the program runs a number of cycles (typically 25 – 50) with charge injection in some channels. The number of ADC counts of each channel and cell is registered and its RMS calculated. This RMS is what will be stored in the data. Variation of the noise level with absorbed dose is not unexpected and is interesting as it obviously affects the signal-to-noise ratio.

Leakage

During the first tests, it was discovered that the radiation caused leakage in the pipeline capacitors of the chip (see chapter 2.2). The program was altered to measure these leakages. The mechanism is the following. Pipeline capacitors are surrounded by two junctions which when irradiated can start to leak. If so, the capacitors will slowly charge up when left idle. To test this, the program resets both a pipeline capacitor and the reference capacitor used for registration of the pedestal. The capacitors are left idle for a certain time after which one of the two is reset and both are read out. Without leakage the value of the two capacitors should be the same if no charge was injected.

Figure 3



Example of plot from ADC ramp test. With constant charge injection, the number of ADC counts registered for a channel (chn 77 of board H7 at 0.5 *Mrad) are plotted against ramp setting.*

Repeating this procedure with different time spans between reset and readout gives a measurement of the amplitude of the leakage current. By choosing which of the two (reference or pipeline capacitor) to reset before reading out them both, one can choose which leakage to measure. If none is reset, we can measure the combined leakage which is the one that might have impact after pedestal subtraction.

6 RESULTS

6.1 PRESENTATION OF RESULTS

After irradiating the three boards to 3.5 Mrad(Si), 6 Mrad(Si) and 3 Mrad(Si), they all continued to operate at full speed which was somewhat surprising. Chip H6 had been brought to 6 Mrad(Si) with the explicit goal of measuring the dose at which it would cease to function. This limit remains unknown. The test procedures described in chapter 5 were developed before the first irradiations but adjusted during the testing of the same board. To verify the results from H3 and H6, the third chip, H7 was irradiated and tested using the accumulated experience to make the process more systematic and precise. All the tests were done within a day after the irradiations and the board was kept in a refrigerator in between irradiations to minimize annealing effects during that time. In this chapter, results from all three chips are given.

Preamplifier Reset Voltage

As mentioned, testing is necessary to study the response to irradiation of an integrated circuit though the behavior of single transistors has been studied extensively and is well known. Honeywell, the manufacturer of the SVX3 chip provides data [11] about the threshold voltage shift of a transistor of the type used in the chip. Comparing their results with our measurements could give an indication of weather our dosimetry analysis was correct or had some important errors and weather the wafer lot that the chips were produced in was outside the expected process characteristics. To do this, we monitored the front end preamplifier reset voltages which is a direct measure of the input transistor threshold voltage. The Honeywell data only gives absolute shift from zero dose voltage and an arbitrary offset has therefore been added to it when comparing with the threshold shifts (fig: 1) measured on chips H3 and H7. The data is found to be in fairly good agreement permitting us to go on with other tests.

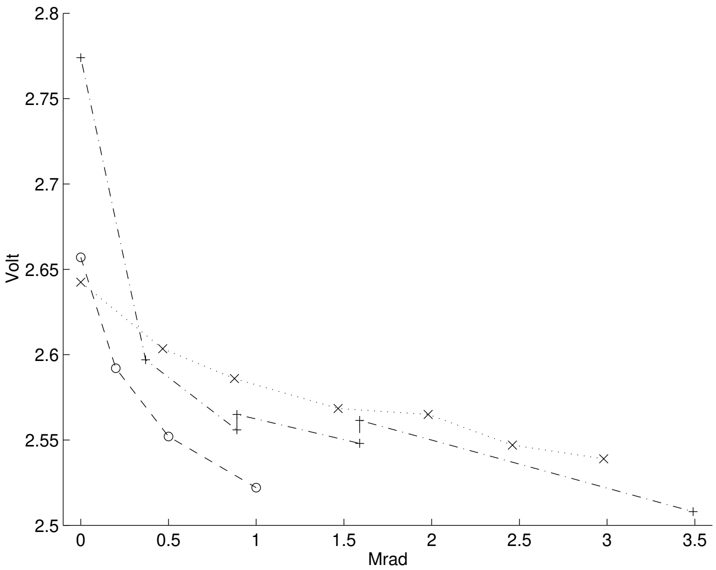
DC Voltages and Currents

As can be observed in figures 2 and 5, the selected bias voltages that were measured showed slopes between 0.5 and 1.9%/Mrad(Si). As mentioned when describing the testing procedure, the monitoring of these voltages primarily can be seen as a probe for symptoms of important changes in the chip.
The measured DC currents (fig: 3 and 4) do not seem to change more than about 20% and we can conclude that power dissipation should not increase in such a way as to justify an adjustment of cooling systems with increasing dose.

Propagation Delays

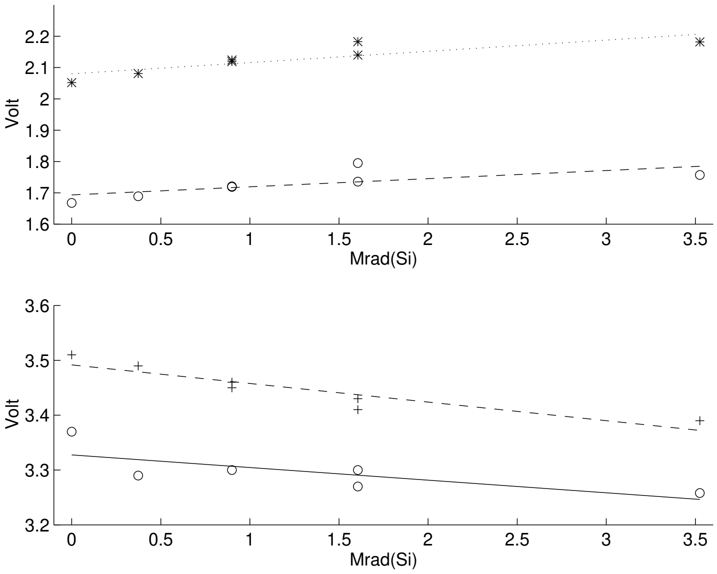
The propagation delays between edges of different digital output signals unfortunately came out somewhat inconclusive. When all measurements on chip H3 and most those of chip H7 were already done, the relatively large scattering of the points led us to go over the way the measurements were made. It turned out that much of the scattering might be due to systematic biases in the measurements. For example the oscilloscope probes used did not all add the same delay, and they may have been swapped in between measurements. Further, the measurements were not all made with the same oscillator frequency on the PATT board and edges of different pulses were used at each measurements. Tests showed all these factors could impact the measurement of a delay by between 0.5 – 2 ns. The first fits made showed different slopes for different chips. However, excluding the first measurement on board H7 when doing the fits was enough for the results to reach a certain agreement in the results (see fig: 6 – 7 and 8 – 9). The data indicates a rise in delays of about 1 ns over 2 Mrad but the data points do not well enough follow the fitted lines to back up such a statement with much certainty. It will

Figure 1



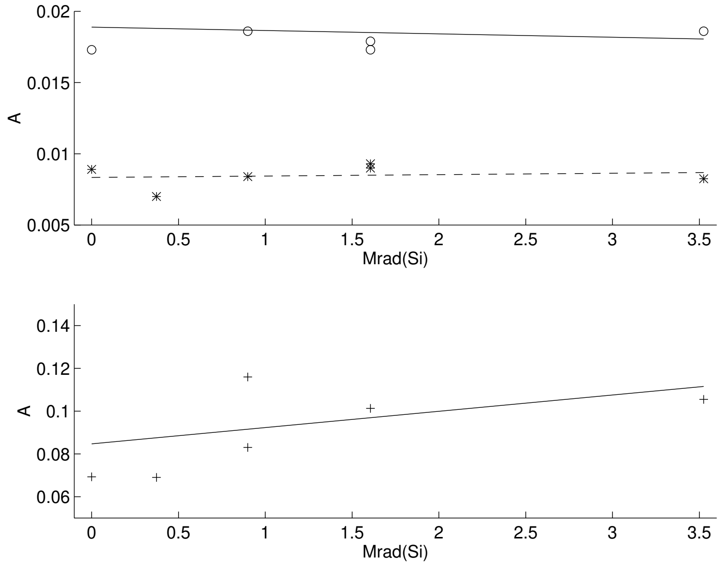
Front end preamplifier reset voltage for chip H3 (+), H7 (×) and data from Honeywell (○) vs. dose. Honeywell data is for p-MOS transistor threshold shift with an added DC offset. Lines are connecting the points to guide the eye.

Figure 2



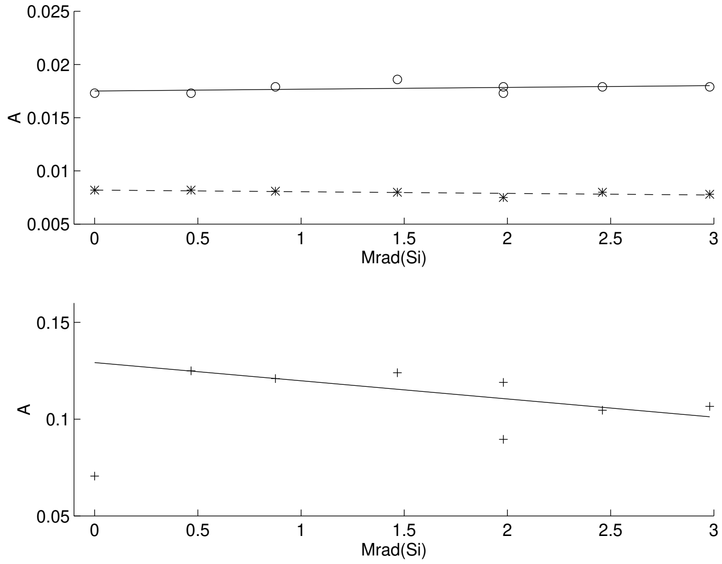
Board H3. Upper plot: Iset1 ○ and dashed line. I quiescent ∗ and dotted line. Lower plot: I drivers ○ and solid line. Iset2 + and dashed line.

Figure 3



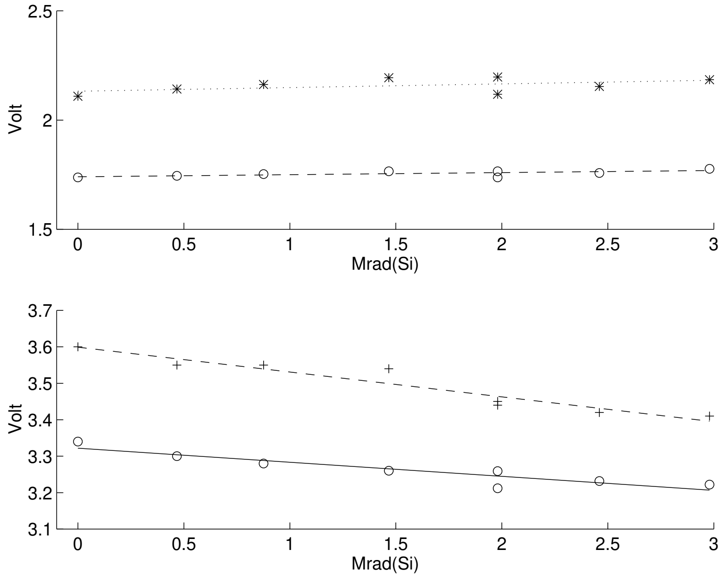
Board H3. Upper plot: AVDD2 ○ and solid line. DVDD ∗ and dashed line. Lower plot: AVDD.

Figure 4



Board H7: Upper plot: AVDD2 ○ and solid line. DVDD ∗ and dashed line. Lower plot: AVDD.

Figure 5



Board H7: Upper plot: Iset1 ○ and dashed line. I quiescent ∗ and dotted line. Lower plot: I drivers ○ and solid line. Iset2 + and dashed line.

be necessary to investigate the variation of these propagation delays thoroughly when testing the next version of the chip as the propagation delays can seriously impact the functionality of the system. Variations in the delays may impact time margins in data readout and require re-tuning in the hardware of the data receivers with increasing dose.

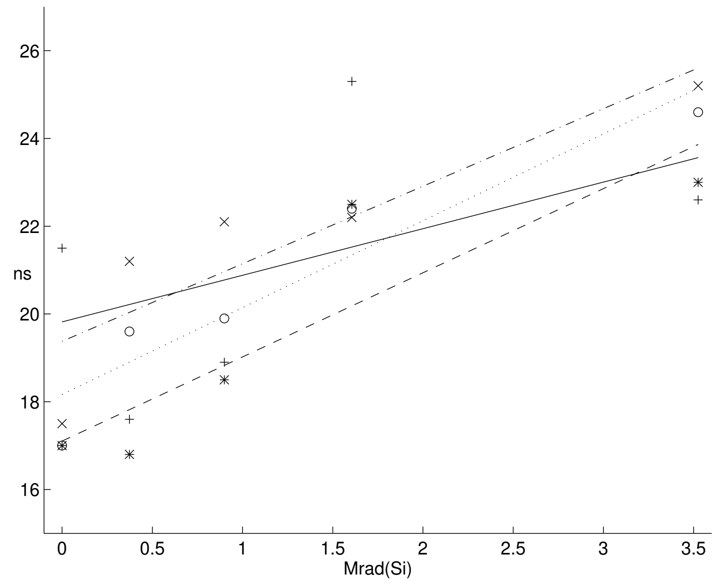
Noise

The zero dose chip noise both measured and calculated by the chip developers to be 800 electrons + 45 electrons/pF of load. The silicon layer receiving the highest dose in the SVX II has a capacitive load of 16 pF and 22 pF (for the ϕ and z strips respectively), and the signal expected for a minimum ionizing particle has a Landau mean of $24,000$ electrons. Therefore the signal to noise at zero dose is 24000/1520 to 24000/1790. Earlier experience with silicon strip detectors shows that as a rule of thumb, a signal to noise ratio of at least 10 is required for efficient pattern recognition. It is therefore important that the signal to noise ratio does not deteriorate very much with radiation. Figure 10 and 11 show the noise variation with absorbed dose for boards H3 and H7. It seems H3 experiences an increase of noise with dose for channels with capacitors of the order of 30%. The noise of H7 does not seem to be noticeably affected until annealing comes into effect when a sudden jump of up to 30% is observed. It seems we cannot rule out an increase in noise with dose with after 2 Mrad(Si) of up to 30%. There is no change in bandwidth and so the signal-to-noise relation will be affected by the same amount as the noise.

Gain

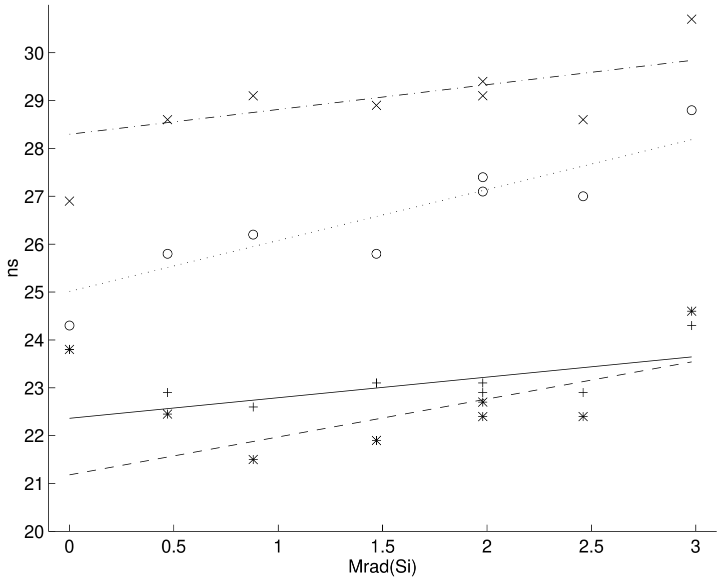
The gain measured in out tests is that the measured gain is that of the full data path including both front and back end is the gain that is measured in our tests. It is a combination of two separate gains. The preamplifier gain in the front end chip and the gain of the ADC in the back end. The preamplifier gain (5 mV/fC) is determined by a ratio of capacitors as long as the open loop gain is high and we therefore do not expected it to change with radiation. However, the measured gain showed a clear dose

Figure 6



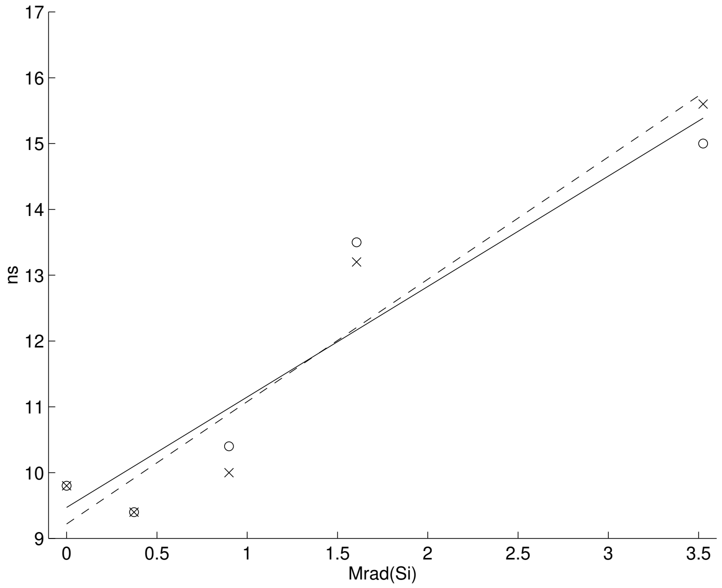
Chip H3: delay between back end clock and data bit zero vs. dose. Rising edge to rising edge: ○ and dotted line. Falling to falling: ∗ and dashed line. Rising to falling: + and full line. Falling to rising: × and dot–dashed line.

Figure 7



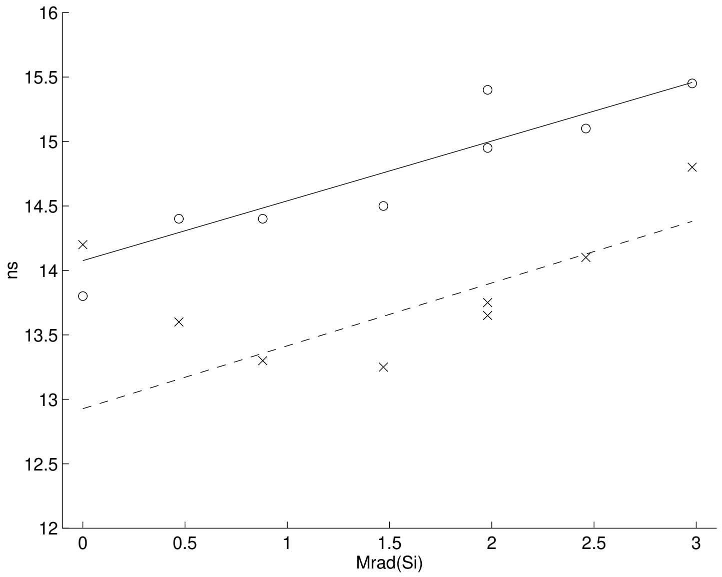
Chip H7: delay between back end clock and data bit zero vs. dose. Rising edge to rising edge: ○ and dotted line. Falling to falling: ∗ and dashed line. Rising to falling: + and full line. Falling to rising: × and dot–dashed line. The first point was excluded from the fit.

Figure 8



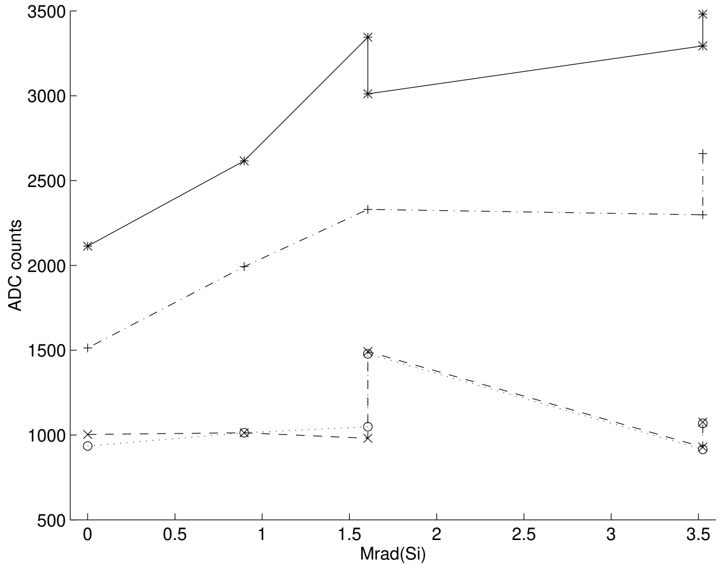
Chip H3: delay between back end clock and data valid vs. dose. Rising edge to rising edge: ○ and full line. Falling to falling: × and dashed line.

Figure 9



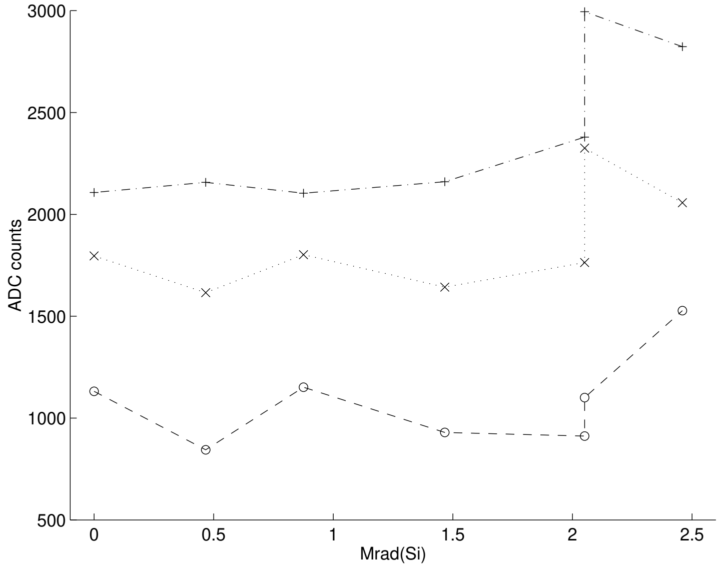
Chip H7: delay between back end clock and data valid vs. dose. Rising edge to rising edge: ○ and full line. Falling to falling: × and dashed line. The first point was excluded from the fit.

Figure 10



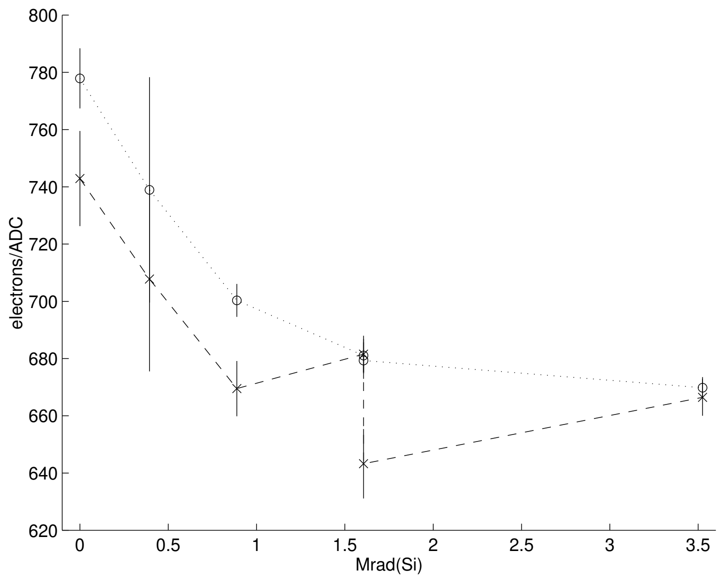
Noise in electrons verses dose for board H3. The noise of four different channels: one loaded with a 10 pF capacitor (+), one with a 22 pF capacitor (∗) and two channels without capacitors (○ & ×). Lines are connecting the points to guide the eye.

Figure 11



Noise in electrons verses dose for board H7. The curves are those of one channel with a 22 pF capacitor (+), one with 10 pF (×) and one without any capacitor (○). Lines are connecting the points to guide the eye.

Figure 12



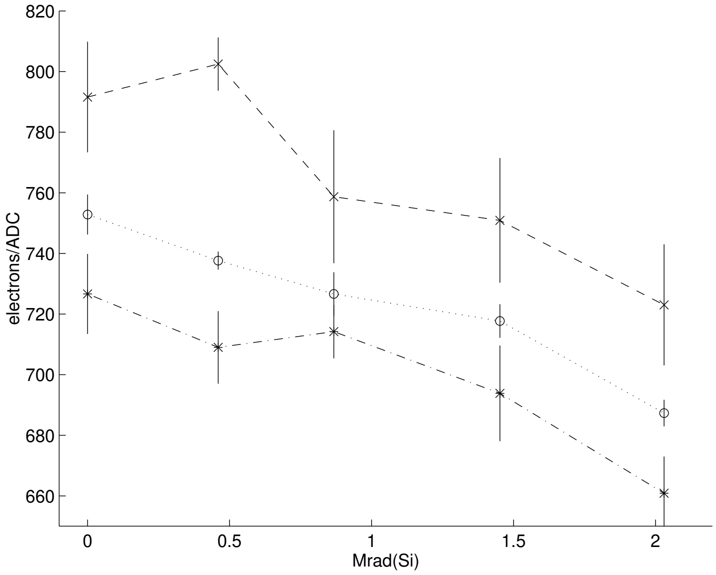
H3: Inverse gain for a channel without capacitor (dotted line) and a channel loaded with a 10 pF capacitor (dashed line). Lines are connecting the points to guide the eye.

dependence (fig: 12 & 13) which probably is due to variations of the ADC ramp rate. This rate is set by a current controlled by the back end ramp rate voltage and an external resistor. The source of this voltage is a diode in a current mirror of which the transistor will experience the same kind of threshold voltage shift as observed for the preamplifier voltage. A plot of the ramp rate voltage shows a dose dependence (fig: 14) confirming our suspicion. When correcting the gain for this variation, we see (fig: 15 and 16) that the gain variations are strongly attenuated further strengthening the hypothesis. The gain will affect both signal and noise equally so the gain rise will not affect the signal-to-noise relation.

Pedestal

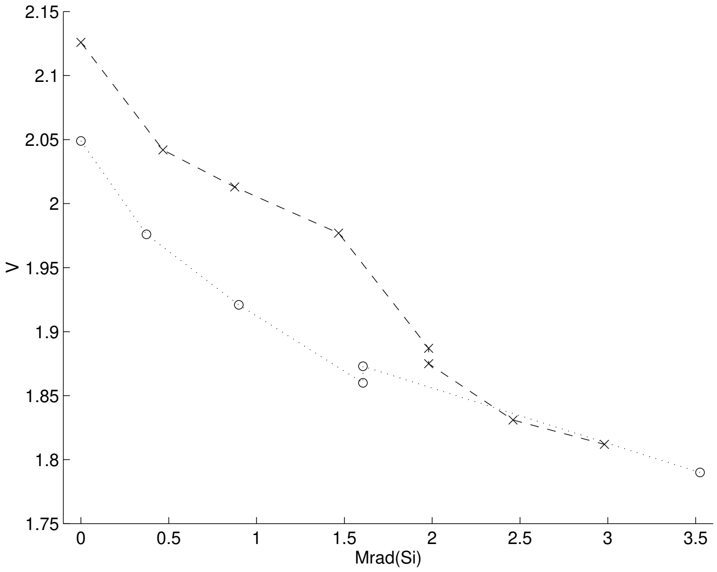
An increased ADC gain should affect the pedestal and the measurements show a clear dose relation (fig: 17) when the average over all cells and channels is plotted versus absorbed dose. Plotting both pedestal and gain together (fig: 18) shows the similar variation of the two and when multiplying the two, we get a pedestal plot with low dose dependence (fig: 19). Efficient usage of the SVX II requires a sparsification threshold level just above the pedestal to register all hits but nothing but the hits in an ideal situation. Any change in pedestal makes this difficult. An over-all change in pedestal level can be compensated for by adjusting the threshold level with increasing absorbed dose. Much worse is a scenario in which large differences in pedestal levels between different channels and cells appear. In such a case, any threshold level will either discriminate hits on cells with low pedestal or constantly register what was no signal on cells with a high pedestal. Two dimensional plots over pedestal verses cell and channel number (fig: 20 and 21) show that the uniformity of the pedestal does not seem to change visibly. To test this more thoroughly, the distribution of pedestal ADC counts (number of channels/cells with a certain number of ADC counts) was calculated. A Gaussian was fitted to the data and the variation of its σ with dose can be seen in figure 22. No real explanation has been found for the bell-shaped form of this curve but it the main conclusion is that σ does not vary by more than 1 count for board H3. The change in average pedestal

Figure 13



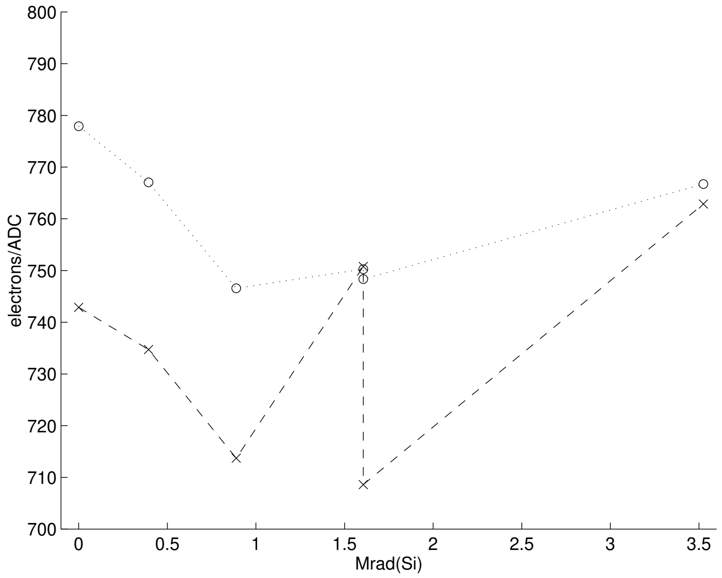
H7: Inverse gain for a channel without capacitor (dotted line), a channel loaded with a 10 pF capacitor (dash-dotted line) and a channel loaded with 22 pF (dashed line). Lines are connecting the points to guide the eye.

Figure 14



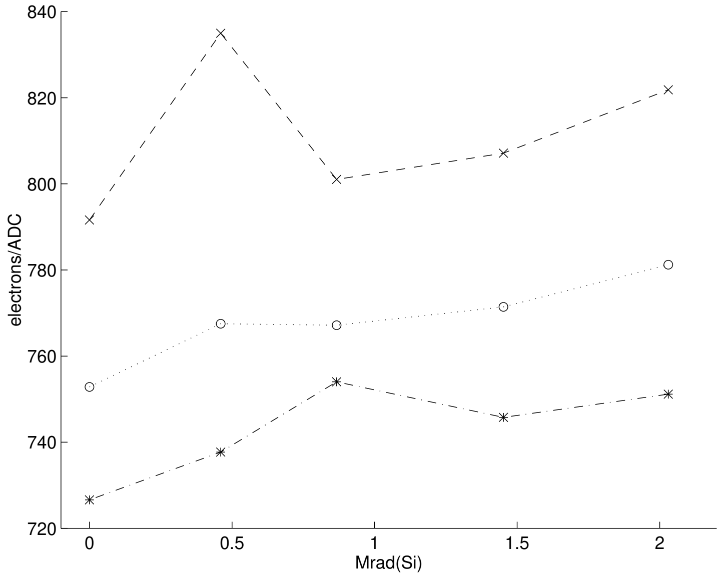
Back end ramp rate voltage verses dose for chip H3 (dotted line) and chip H7 (dashed line). This voltage controls the ramp of the ADC thereby affecting the gain. Lines are connecting the points to guide the eye.

Figure 15



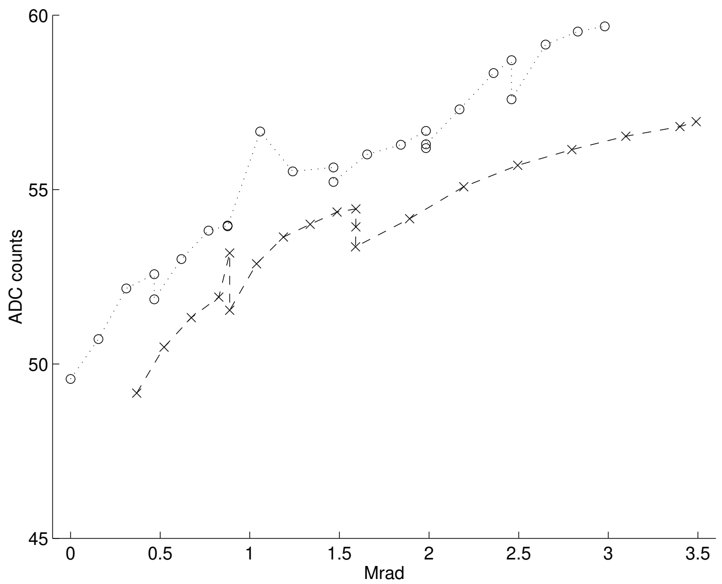
H3: Inverse gain for the same two channels as in figure 12 but corrected with a factor corresponding to the relative change in ramp rate voltage. Lines are connecting the points to guide the eye.

Figure 16



H7: Inverse gain for the same three channels as in figure 13 but corrected with a factor corresponding to the relative change in ramp rate voltage. Lines are connecting the points to guide the eye.

Figure 17



Pedestal for boards H3 (dashed lines and ×) and H7 (dotted line and ∘) verses absorbed dose. Lines are connecting the points to guide the eye.

is about 10 counts or 20% and it seems clear that it really reflects a change in all-over pedestal level. Both gain and pedestal variations are linked and mainly explained by the changes in ramp rate voltage which is understood. A pedestal variation does not affect the signal to noise ratio as it is really a value first added and then subtracted to the signal. However, efficient usage of the SVX II requires a sparsification threshold level just above the pedestal to register hits but nothing else in the existent this is possible. A varying pedestal implies that the threshold level must be adjusted during the run.

Pipeline Delay

The testing of the pipeline delay did not work for all chips. However, it did not seem to be affected by absorbed dose. H3 and H6 passed the test without problems at all doses whereas the program could not be made to work with chip H7 at all.

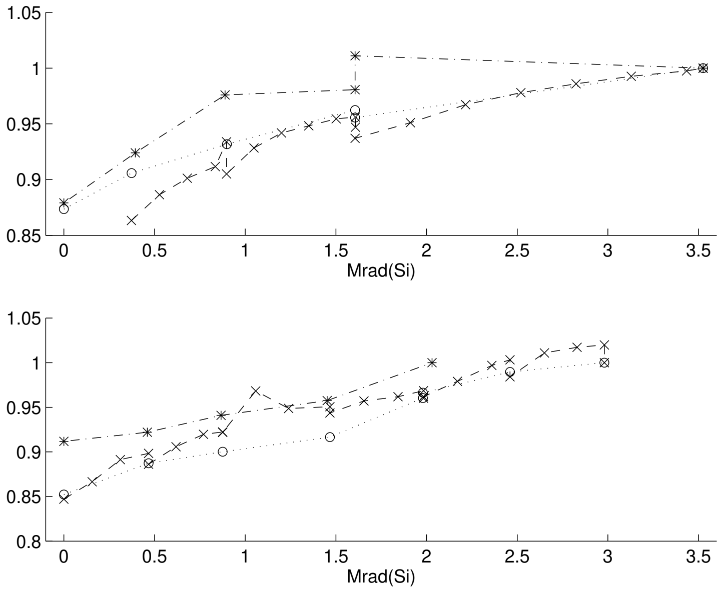
Rise Time

The data collected during the irradiations was used to calculate 10% – 90% rise times as well as the time constant of the different rise times. For a single channel, neither seemed to vary notably.

Leakage

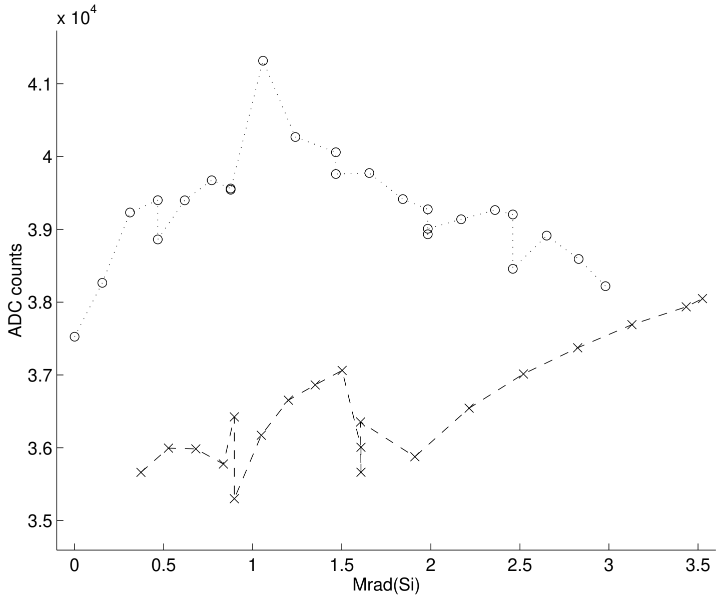
The leakage of the pipeline capacitors was totally unexpected and showed up after the first irradiation as semi-periodical peaks in the values readout from the chip. About every 40 ms, the otherwise relatively stable value read out from a certain cell suddenly had a peak only to return to normal values just after (fig: 23). The explanation for this fenomenon is that probably leakage of the pipeline capacitors occurs but in normal operation the capacitor does not have time to charge up notably. At times, however, the computer used for the test in question paused to flush data from the active memory to the hard disk creating an unexpected time span during which no control signals were given and the capacitors were left idle giving them opportunity to charge up. The test

Figure 18



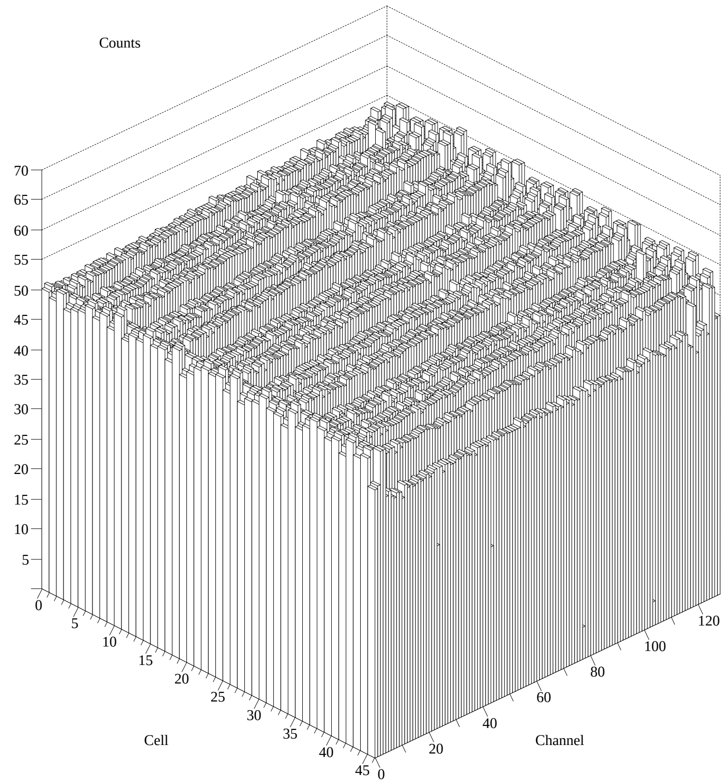
Upper plot: board H3. Lower plot: board H7. Pedestal (dashed line), inverse of ramp rate voltage (dotted line) and gain (dot-dashed line) in one plot verses dose to show the dependence of the three. Data of all curves have been normalized to reach one at the last point. Lines are connecting the points to guide the eye.

Figure 19



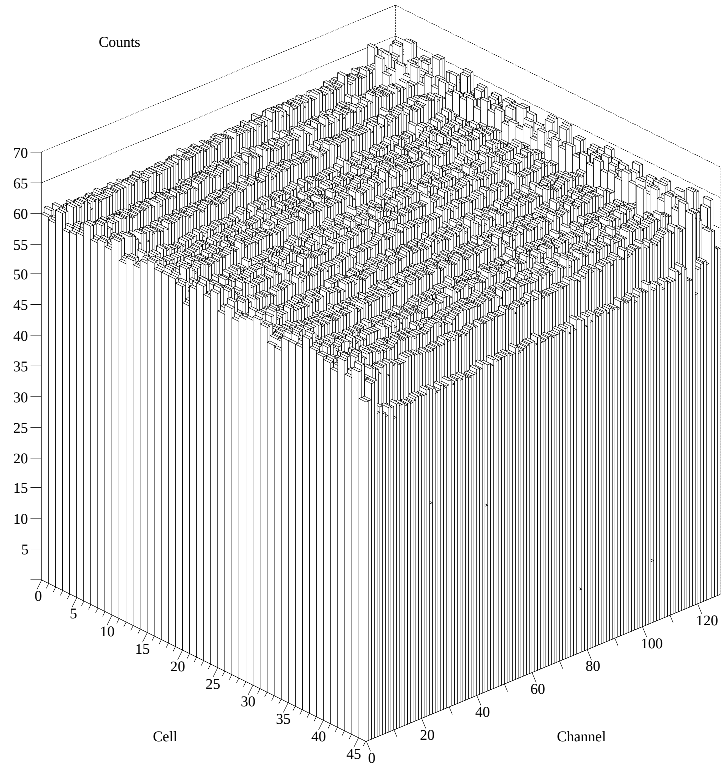
Pedestal for boards H3 (dashed lines and ×) and H7 (dotted line and ∘) times gain verses absorbed dose. Lines are connecting the points to guide the eye.

Figure 20



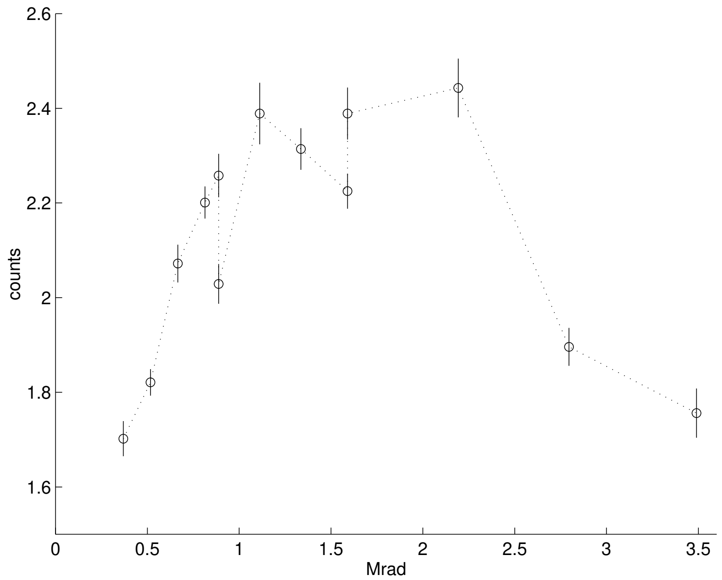
Plot of the pedestal for each cell / channel of board H7 at 0 Mrad(Si).

Figure 21



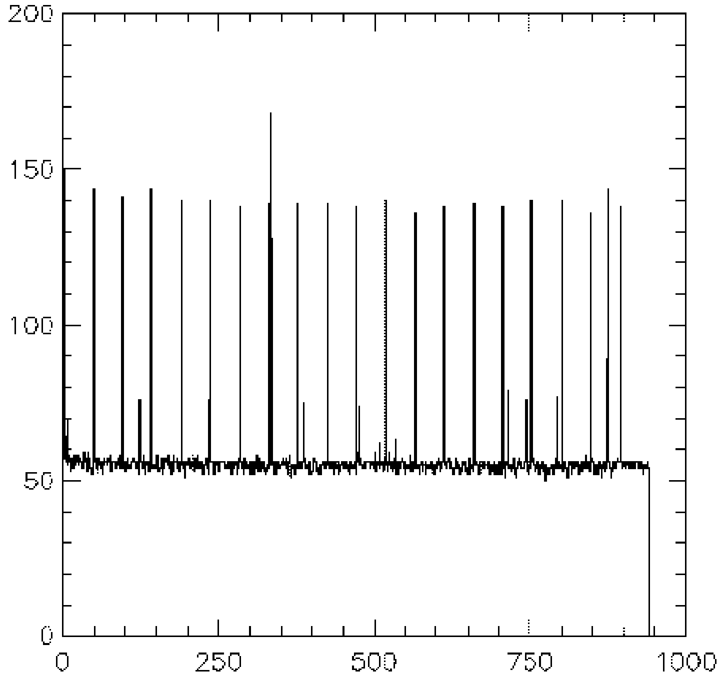
Plot of the pedestal for each cell / channel of board H7 at 3 Mrad(Si) after annealing.

Figure 22



Board H3: σ of Gaussian fit to the distribution of counts for the pedestal of all channels and cells vs. absorbed dose. Lines are connecting the points to guide the eye.

Figure 23



ADC counts from repeated readouts of one cell of chip H3 without charge injection verses time in milliseconds. The high peaks are believed to be due to leakage in the pipeline capacitors made visible during pauses imposed by the operation of the computer.

procedure then set up for further irradiation showed that the effect is measurable only for times of the order of a millisecond while normal operation is expected to allow pauses of at most 50 μs. As a representative case, the rate of pedestal shift due to the leakage in the reference capacitor of one channel is given as function of dose in figure 24. The largest rate of shift observed, 25 counts per millisecond would lead to a mere 1 count shift after 50 μs.

Ramp Pedestal

The gain variations are expected to slightly affect the ramp pedestal plot by stretching it slightly but this effect is barely visible on the plots.

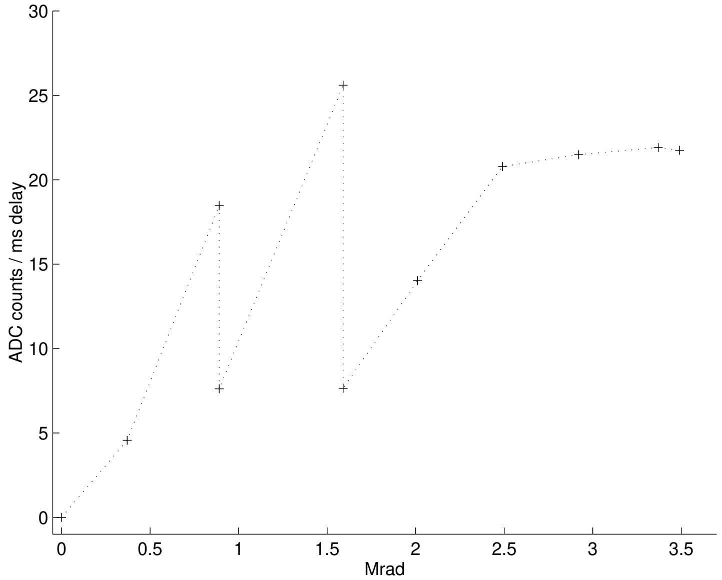
Rise Time

The rise time of the input preamplifier can be set with a variable in the range 0–7 to obtain optimal signal-to-noise relation for the used integration time which in its turn is limited by the bunch crossing time of the accelerator. Rise time plots for a channel loaded with a capacitor for doses from 0 to 3.5 Mrad(Si) show (fig: 25) no visible dose dependence nore for bandwidth setting 7. A change with dose of the rise time could have affected the signal-to-noise relation.

6.2 ERRORS

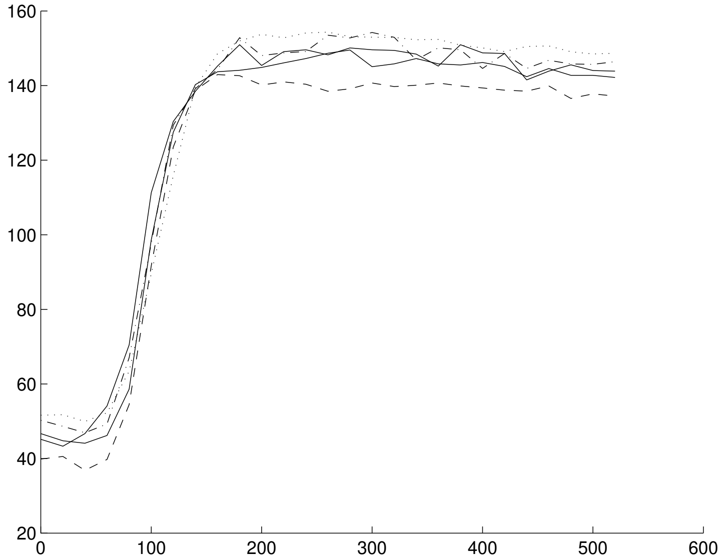
The dominant uncertainty in this study comes from the dosimetry. In chapter 4, several sources of error were mentioned. When combining them all together (see table 26), a total error of 15% that affects all dose measurements. We have assigned a 10% error to

Figure 24



Rate of pedestal shift due to leakage of the reference capacitor of one channel as function of absorbed dose. More than one point at the same dose indicates that annealing took place between them. The points are connected in order of increasing time.

Figure 25



Rise time plot for the input transistor of board H3 for doses ranging from 0.3 Mrad(Si) to 3.59 Mrad(Si). A channel loaded with a 10 pF capacitor has been chosen and bandwidth setting is 7.

Table 26 **Errors connected with dosimetry.**

Source	*Error*
TLD Dose measurement	9%
Chip positioning	3%
Charged particle equilibrium*	9%
Low energy gamma rays*	3%
Total error	15%

* Correlated errors.

possible lack of CPE based on data for dose enhancement effects near interfaces [4] for the 1.25 MeV rays and 30% for the 0.2 MeV ones. When calculating the dose received by the chip during the different irradiations, only the chip positioning error of 3% will be statistical. The remaining enter only in the determination of the intensity of the source of 505 MeV(Si)/min and are common.
The reader might have noted that only a few of the figures carry error bars. Most of the figures with data taken on-line are based on large event samples leading to negligible statistical errors. The equipment used to measure voltages and currents has negligible measurement errors.
The propagation delays (fig: 6 and 7) on the other hand, have a ± 1 ns measurement uncertainty and the procedure used to define edge crossings varied during the study contributing with an additional $2 - 3$ ns systematic uncertainty. Some of the earlier delay measurements for board H3 were done with a 50 MHz clock running instead of the 10 MHz clock used later. No error bars are shown for the delay points, but the observed scatter is indicative of these uncertainties. The points may have additional systematic biases due to i.e. the oscilloscope probes used as discussed in chapter earlier. The exclusion of low dose points that were done before a routine was established make the data from different chips agree. Although the data is not very convincing, the obtained agreement can serve as an indication of probable behaviour. However, some signals have critical timing within the chip for the version tested, and so it is possible that the observed scatter is real.
The uncertainty concerning the gain, and therefore also the noise, is dominated by our knowledge of the SVX3 internal calibration capacitances which carries a 10% error. This is a correlated systematic uncertainty which affects normalisation of plots but not their shape vs. dose.

7 SUMMARY AND CONCLUSION

After irradiation up to 6 Mrad(Si), the SVX3 chips that were tested continued to work at full speed. The features that are affected by the dose experience changes that should not cause problems for the operation of the chip during Run II. No adjustments of equipment with increasing dose should be necessary, with the possible exception of the timing of the data receivers. The obtained results suggest that this might be necessary but are inconclusive due to the suspected high uncertainties in the measurements. Further study is obviously necessary to investigate this. It would be good to carefully monitor the effects of radiation on data delays on the next version of the chip.

The rise in gain will require tuning of the sparsification threshold level because of the increase in pedestal it leads to. A noise rise of about 20% can be expected when approaching 2 Mrad(Si), affecting the signal-to-noise ration by the same amount since there is no observed change in bandwidth.

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A MISCELLANEOUS

A.1 ACCELERATOR PHYSICS

A.1.1 Luminosity

In a colliding beam experiment as the CDF, there will be interactions of many different kinds The luminosity $\mathcal{L}$ of a reaction for example $p\bar{p} \longrightarrow t\bar{t}$ is the frequency of such interaction per cross section surface area. If we assume that N_p, $N_{\bar{p}}$ are the number of protons and antiprotons, f is the frequency of collisions and $\sigma_x\sigma_y$ is the transverse area of the collision, we have

$$\mathcal{L} = \frac{N_{\bar{p}} N_p f}{4\pi\sigma_x\sigma_y} \quad \left[\frac{1}{\mathrm{cm}^2\mathrm{s}^1}\right] \tag{A.1}$$

This luminosity is also called instantaneous luminosity as opposed to the integrated luminosity which is simply the integral of $\mathcal{L}$ over the time of the experiment. To calculate the number of interactions, simply multiply by the cross section:

$$N_t = \sigma_t \int \mathcal{L}\, dt \tag{A.2}$$

In Run II of CDF, one expects $N_t = 10^4$ and about 100 detected top events.

A.1.2 Collision Energy

The energy in a $\bar{\mathrm{p}}\mathrm{p}$ collisions is given as $\sqrt{s}$ where s is given as

$$s = (P_{\bar{p}} + P_p)^2 \tag{A.3}$$

Where P are the 4-momenta of the respective particles.

A.2 BRIEF OVERVIEW OF THE STANDARD MODEL

The standard model is today the broadly accepted theoretical model describing the subatomic structure of matter. According to this model, the world we know is built up by particles (leptons and quarks, see table 1) and three forces mediated by bosons. The particles we encounter are either the leptons (i.e the electron) or hadrons made out of combinations of two or three quarks. The forces acting between particles are the commonly known electromagnetic force mediated by the photon, the strong and the weak forces using Z / W bosons as mediators. The elementary particles are divided into three generations (see table: 1) that have great similarities. Basically, the mass is the main difference between them. The μ is for example mainly a heavier version of the electron. The particles were found family by family and the finding of the top quark marks the end of the search for particles with which to fill the blanks in the table. From now on, particle physics will more and more direct itself towards search for the physics beyond the standard model i.g supersymetry.

Table 1 **Elementary particles**

	Leptons		Quarks	
First Generation	e	ν_e	u	d
Second Generation	μ	ν_μ	c	s
Third Generation	τ	ν_τ	b	t

B IRRADIATION LOGS

A total of three chips manufactured by Honeywell were irradiated. They were numbered H3, H6 and H7 in the order of assembly. As seen in the tables below, the radiation effects were at ocasions let to anneal in an oven set at 100°C.

Table 1 **Irradiations of board H3**

Number	Dates	Exp time (min)	Total dose
3.1	9–10 October	738	3.72 Mrad(Si)
3.2	28–29 October	1038	8.97 Mrad(Si)
		Annealing one day	
3.3	30–31 October	1409	1.61 Mrad(Si)
		Annealing one week	
3.4	12–15 December	3805	3.53 Mrad(Si)
		Annealing one day	

Table 2 **Irradiations of board H6**

Number	Dates	Exp time (min)	Total dose
6.1	31–3 Oct/Nov	3689	1.86 Mrad(Si)
		Annealing five day	
6.2	16–19 January	3910	3.83 Mrad(Si)
6.3	23–26 January	3850	5.78 Mrad(Si)

Table 3 **Irradiations of board H7**

Number	Dates	Exp time (min)	Total dose
7.1	9–10 January	924	0.47 Mrad(Si)
7.2	14–15 January	810	8.76 Mrad(Si)
7.3	19–20 January	1170	1.47 Mrad(Si)
7.4	22–23 January	1023	1.98 Mrad(Si)
		Annealing one week	
7.5	4–5 February	936	2.46 Mrad(Si)
7.6	11–12 February	1032	2.98 Mrad(Si)
		Annealing four days	