The SVX3D Integrated Circuit For Dead-timeless Silicon Strip Readout

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Abstract

The revision D of the SVX3 readout IC has been fabricated in the Honeywell radiation-hard 0.8μm bulk CMOS process, for instrumenting 712,704 silicon strips in the upgrade to the Collider Detector at Fermilab. This final revision incorporates new features and changes to the original architecture that were added to meet the goal of dead-timeless operation. This paper describes the features central to dead-timeless operation, and presents test data for un-irradiated and irradiated SVX3D chips.

1 Introduction

A mixed signal integrated circuit denominated SVX3D has been developed to instrument the silicon strip sensors (712,704 channels) of the upgrade to the Collider Detector at Fermilab [1]. It has been fabricated in the 0.8μm bulk CMOS radiation hard Honeywell process. Each IC contains 128 parallel analog inputs and an 8-bit digital output bus.

The SVX3 architecture has been previously described at various stages of development [2,3]. This paper concentrates on the features critical to dead-timeless operation, which have evolved substantially since the first SVX3 prototype. The term dead-timeless refers to the continuous acquisition of analog signals, even while previously acquired signals are being held and/or digitized, or during transmission of data on the output bus.

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Although the implementation has evolved, the performance goals have not changed since the original design.

(1) Low noise integration of either positive or negative charge from AC-coupled silicon strips (signal to noise must be better than 10:1 for minimum ionizing particles), with variable integration time between 100ns and 360ns and no more than 3.5mW/channel power consumption [4].
(2) Parallel sampling of each analog input at a rate of up to 7.6 MHz, and storage of all samples for up to 5.5 μs.
(3) 8-Bit digitization of arbitrary samples for all channels in parallel together with sparse readout of digitized signals, all at an average rate of up to 40 KHz with zero dead-time.
(4) Radiation hard up to a low rate accumulated dose of 2 MRad.

While problems (1), (2) and (4) have been previously solved [5,6], the design and implementation of these existing solutions had to be fundamentally changed in order to also meet condition (3).

Condition (2) was met in ref. [6] using an “analog pipeline”, consisting of a voltage amplifier and a switched capacitor array. For SVX3 the same principle is used for short term storage of analog samples, but in this case two amplifiers and double the number of switches are needed. Complex control logic is also required to manage continuous storage of new samples using one amplifier, even while old samples are queued for digitization or being transferred to the ADC using the second amplifier. The SVX3 pipeline is described in detail in ref. [2] and will not be discussed further here. The implementation in the SVX3D IC has not changed significantly from earlier prototypes.

2 The Charge Integrator

The SVX3D charge integrator is a cascode amplifier with n-MOS input transistor [7]. This is different from refs. [5] and [6], and even from the original SVX3 design, all of which used p-MOS input transistors. The advantage of the former is that the amplifier is relatively insensitive to noise on the drain voltage (AVDD). The immunity to AVDD noise is vital for dead-timeless operation because in a dense package it is difficult to keep the AVDD power supply quiet while the digital output bus is active. Measurements on SVX3 revisions that had a p-MOS input transistor showed that a 1 mV step on AVDD produced a response at the integrator output equivalent to $19,000$ e of input charge. By contrast for SVX3D a 1 mV step on AVDD is equivalent to just 600 e of input charge. The reason for the better noise rejection is that regardless of the input transistor kind, the gate always has a parasitic capacitance to the the substrate due to the amplifier input trace, bonding pad, and

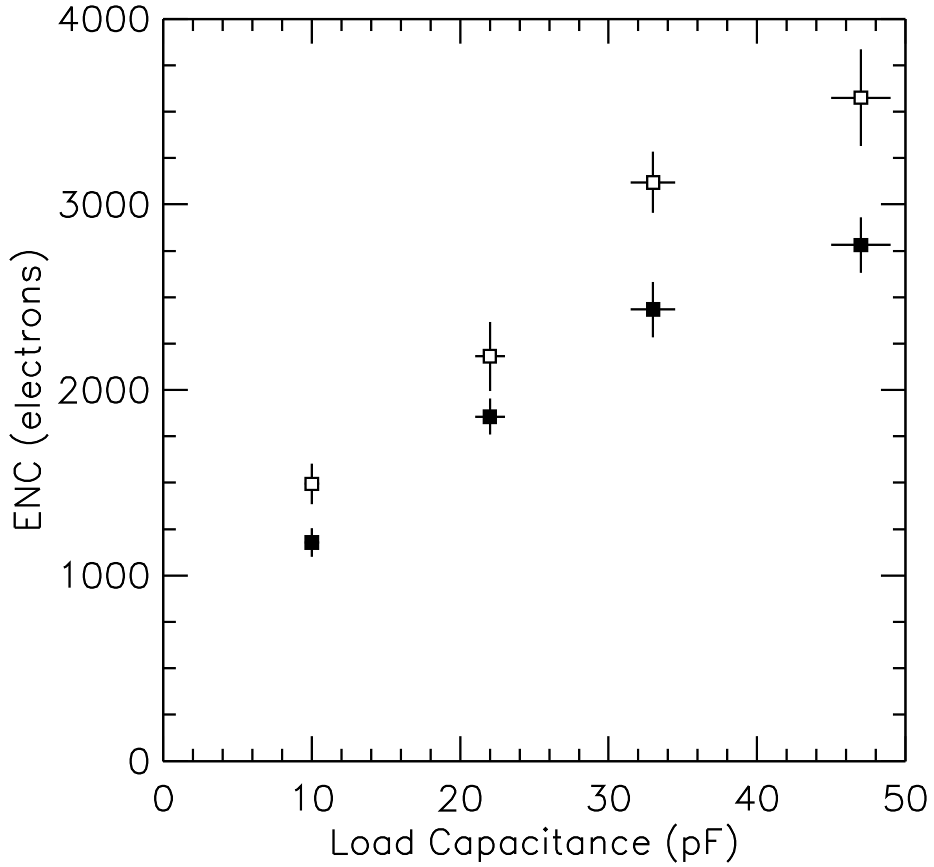

Fig. 1. SVX3D equivalent noise charge vs. input capacitance before (solid) and after (open) 3.8 MRad irradiation. In all cases the 0-90% rise-time of the integrator is approximately 60 ns.

protection diodes. In order to avoid spurious charge injection by this parasitic capacitance, the input transistor source must be referenced to the substrate, which is the case for an n-MOS input transistor (where the substrate is the IC ground as explained in the next section).

A consideration against the use of an n-MOS input transistor was the possibility that the noise performance would deteriorate faster with accumulated radiation dose than for p-MOS devices [8]. Irradiation tests have now been carried out up to 4 MRad doses and the noise performance of SVX3D is acceptable. Figure 1 compares noise before and after 3.8 MRad Co^{60} exposure for various capacitive loads. The noise increases after exposure by a factor of 1.26 ± 0.08. The integrator rise-time is adjusted for each measurement to between 60 ns and 70 ns (0-90%), and a 120 ns integration time is used. The rise-time is adjusted by selecting (via on-chip registers) different capacitance values for the pole of the amplifier circuit. This does not affect the input transistor current, which is 190 μA in all cases. The discrete nature of

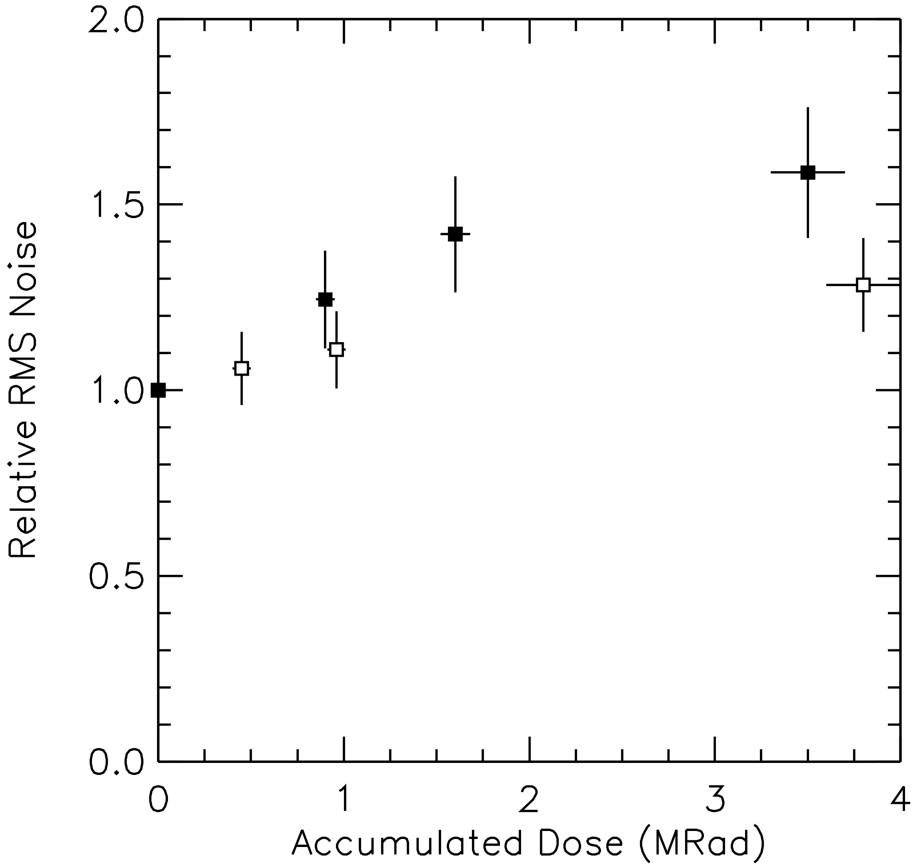

Fig. 2. Comparison of SVX3D (open) and SVX3B (solid) relative noise increase vs. radiation dose. Data from various capacitive loads have been combined assuming that the noise after dose d is given by a load-independent scale factor $F(d)$ times the noise at zero dose. The 0-90% rise-time for all measurements was approximately 60 ns. The SVX3D IC has an n-MOS input transistor, while the SVX3B IC has a p-MOS device.

the adjustment introduces small systematic deviations from a straight in the points in Figure 1. Figure 2 compares the noise increase with accumulated dose to data from revision B of the SVX3 IC [9], which was manufactured in the same process but had a p-MOS input transistor. The exposure rate was 500 Rad/min, and 100^{o}C annealing steps were interleaved with exposures in an attempt to more closely reproduce the effects of low dose rate damage [10].

3 Dead-Timeless Operation

Digital switching is present in the operation of any mixed signal device, even during "purely analog" operations such as charge integration, where switches have to open and close to start and end the integration period. However, normally all switching can be synchronized to some fixed phase of the analog activity, thus resulting in arbitrary but constant pedestal offsets. But synchronization is not possible for dead-timeless operation, because data must be transmitted simultaneously with analog activity, and the data values are neither constant nor known in advance. In this case one must isolate the digital and analog functions, so that digital switching can take place without influencing the outcome of analog operations.

The mechanisms than can couple digital switching to analog operations can be classified in terms of the three media that can be involved.

(1) Substrate.
(2) Package.
(3) Environment.

The sensitivity of the front end integrator to power supply noise discussed in the previous section belongs to the package category. Dense packaging will inevitably introduce capacitive coupling between signals, power and ground, and while the importance of "good" package design to minimize coupling and provide effective by-passing cannot be over-emphasized, it is just as important for dead-timeless operation to have circuits that are immune to low levels of power supply noise.

To address substrate coupling mechanisms, the original SVX3 design consisted of two separate ICs, one with the integrator and analog pipeline, and another with the ADC and digital I/O. However, both ICs were fabricated in the same technology, on the same wafer even, and the division was inconvenient due to the required high density wirebond interconnection, and the difficulty of probing separate devices that are supposed to work together. SVX3D is a single IC and, though counter-intuitive, substrate coupling is avoided by exploiting the low resistivity of the substrate.

The Honeywell bulk CMOS radiation hard process uses a low resistivity substrate. Normally, this choice of substrate is problematic for mixed signal ICs, because the substrate is referenced to ground through wirebonds and IC package pins that together have non-negligible resistance and inductance. In this case a digital current returning to ground through the substrate (via capacitive coupling) will develop a potential drop in the IC, and thanks to the low resistivity of the substrate the analog sections of the IC will "see" this potential drop.

In SVX3D, analog ground connections are made directly through the substrate. No wirebonds or pins are involved. The die have been thinned and back-metalized, and are mounted with conductive epoxy onto the system ground plane. The contact resistance between the substrate and the ground plane has been measured to be under 1 mΩ. Thus the substrate of the IC becomes the system ground, and currents returning to ground have only to cross a few microns of the high resistivity epilayer that the circuitry is built on. Any two points on the IC separated by a distance large compared to the thickness of the epilayer are thus isolated.

Coupling mechanism (3) involves pick-up of fluctuating electro-magnetic (EM) fields created by digital clocks and data transmission (environment noise), but the IC by itself is physically too small to be sensitive to EM fields of this magnitude. Therefore, by not connecting the IC analog inputs one is able to study mechanisms (1) and (2) independently of (3). Further discussion of environment noise is postponed until section 5.

4 Performance

Pedestal stability is taken as the critical indicator of dead-timeless performance. It is imperative that the pedestal of analog samples not change with time as digital operations take place simultaneously with analog acquisition. The reason is that only "hit" channels will be read out by the data acquisition system (sparsification), and the discrimination of hit from non-hit channels is based on a comparison of the digitized signal level of each channel with a programmable but fixed sparsification threshold.

To characterize pedestal stability a "pedestal map" is constructed for a given channel (Fig. 3) as follows. The device under test (DUT) is exercised by running repeatedly a fixed control pattern. The pattern begins with an initialization step, so that the same sequence of operations is repeated by the DUT on every run. Following initialization, the pattern makes the DUT acquire 201 consecutive analog samples (numbered 0 to 200) with a period of 140 ns. Any one but the first of these samples can be selected by a programmable trigger for digitization and readout after the end of the run. Thus every run yields an ordered pair of data for each channel of the DUT: [sample number, ADC count]. To produce a pedestal map the sample number is varied between 1 and 200 by changing the programmable trigger position from run to run. At least 200 runs would therefore be needed in order to produce Fig. 3. In practice 6,000 runs went into making Fig. 3 in order to discern systematic pedestal variations from random integrator noise.

Simultaneously with the acquisition of samples, the control pattern walks the DUT through various digital operations. A fixed trigger is always given to select sample 0 for digitization and readout. This is a dummy sample that cannot be selected by the programmable trigger and is not used to construct the pedestal map. For the remainder of the first 72 samples there are no

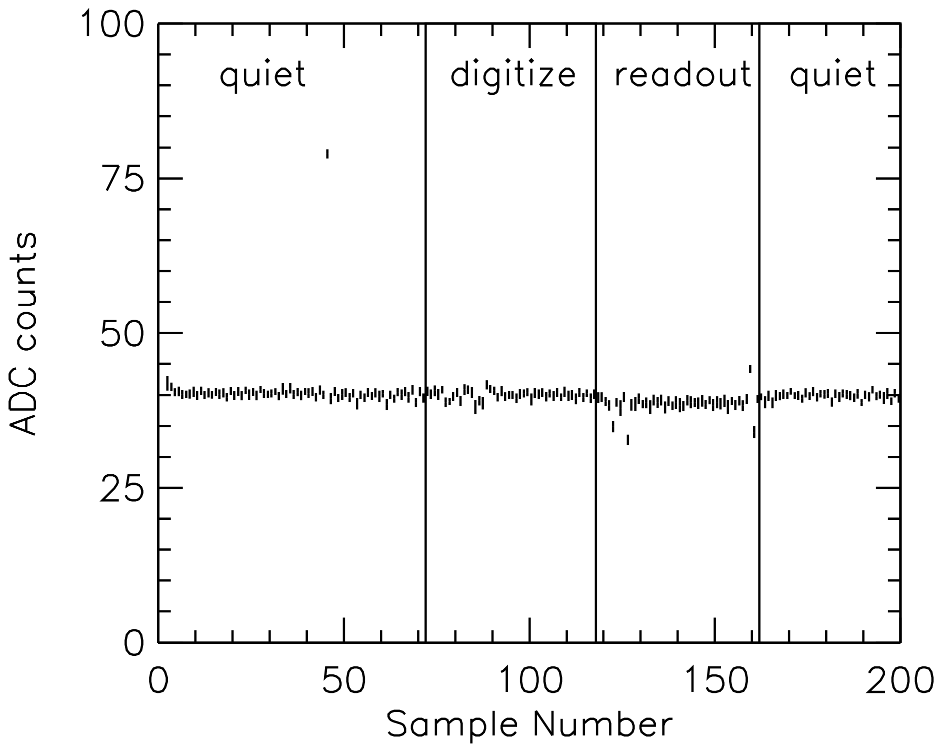

Fig. 3. Pedestal map for a single channel of an SVX3D IC mounted on a prototype hybrid circuit board. Each point is an average of 30 samples, with the error bars showing the RMS spread. The vertical scale is in ADC counts, with 1 count corresponding to approximately 600 electrons of input charge.

additional operations. We refer to this as a "quiet" operation mode (equivalent to the acquisition mode of ref.[6]). During samples 73 to 117 the selected dummy sample is digitized, and during samples 118 to 162 the resulting data are transmitted on the output bus (readout), and later discarded. Note that the programmable trigger that selects the samples used to produce the pedestal map is independent from the fixed trigger that selects the dummy sample. If for a given run the programmable trigger happens to select sample 2, for example, this sample will be queued for digitization at the end of the pattern, and will not interfere with the digitization and readout of the dummy sample.

Fig. 3 was constructed using an SVX3D IC mounted on a prototype hybrid package with the highest density and minimum bypassing that will be present in the CDF-II silicon detectors. With the exception of samples 44, 122, 126, 159, and 160, it shows that the pedestal is stable at the level of two ADC counts, which corresponds to 1,100 electrons of input charge. This is adequate for dead-timeless operation as it is smaller than the integrator noise (see Fig. 1). In sample 44 approximately 4 fC of input charge was injected using a calibration circuit, in order to show a typical signal. The remaining samples 122, 126, 159, and 160 show real pedestal fluctuations during data readout. Additionally, sample 156 (which does not look abnormal) contains invalid data due to a pipeline reset operation performed at that point in the pattern. While the pedestal map is a valuable performance bench-mark, it is not an exhaustive test of all possible sources of pedestal shift, and other studies are needed before successful dead-timeless operation can be claimed.

5 Environment Noise and Real-Time Pedestal Subtraction

The previous sections showed how substrate and package coupling problems have been overcome in SVX3D, resulting in a device that has good dead-timeless performance in a "clean" bench-test environment. However, a silicon strip connected to an integrator input will act as a sensitive antenna for environment noise. From the standpoint of a single channel all charge originating in the silicon sensor is by definition signal, whether its cause is a charged particle penetrating the sensor or "pick-up" of fluctuating EM fields.

The SVX3D IC has a differential balanced current design for the digital output bus in order to minimize the source of fluctuating EM fields during readout. Each differential output contains an adjustable current source and a matched current sink, so that the operating voltage swing can be varied given a termination resistance. This reduces, but does not eliminate environment noise. At this point it is up to the detector design to incorporate shielding on cables and circuits carrying digital signals in order to achieve any further reduction. This presents a challenge for dead-timeless operation because of the need to balance shielding with mass and space constraints, and the practical impossibility of evaluating ahead of time the level of environment noise given a very complex geometry.

In order to add a safety margin to the tolerable level of environment noise, a new real-time pedestal subtraction (RTPS) circuit has been implemented in SVX3D [11]. As stated before, there is no way for the circuitry of a single channel to distinguish pick-up of environment noise from signals of actual charged particles penetrating the silicon sensor (hits). However, using all 128 channels in the IC it *is* possible to distinguish them given two simple conditions.

(1) Low hit occupancy (this is the same condition that makes data sparsification viable).
(2) Uniform pick-up of environment noise by most of the 128 channels.

The new circuitry uses all channels to calculate (in real time) a common pedestal and subtract it from each channel during digitization, before sparsification takes place. This is equivalent to making the sparsification threshold a dynamic variable that tracks common-mode pedestal fluctuations.

Condition (2) is crucial for the RTPS circuit to function, but it is not obviously true. It is certainly possible to induce local pedestal fluctuations by running un-shielded digital signals over one part of the silicon sensor and not another. However, studies carried out with prototype detector modules [12] showed that with minimal shielding (not enough to eliminate environment noise), even signals running over silicon sensors produced uniform pedestal fluctuations. Therefore, while eradicating environment noise with shielding and geometry remains a great challenge, avoiding localized EM field fluctuations is straightforward.

Regarding condition (1), in bench tests RTPS performs well with occupancies as high as 60%. Typical occupancies in particle physics detector applications vary depending on geometry and accelerator environment. For the Collider Detector at Fermilab the maximum occupancies in strips parallel to the colliding beams are of order 10%, whereas for strips perpendicular to the beam direction they are predicted to occasionally reach 60% and higher. However, 128 adjacent hits strips (100% occupancy) provide no position information, and it is therefore expected that a degraded ADC performance for extremely high occupancies would have no adverse effect on track reconstruction.

The implementation of the RTPS circuitry is simple in the context of the pre-existing Wilkinson ADC design. The ADC is a voltage to time conversion (v-t), where time is measured in number of cycles of an externally supplied clock using a Gray code counter. The v-t conversion is done by presenting the voltage to be converted, V_i, at the input of a comparator, and supplying a linear voltage ramp, $V_r(t)$, to the other input. The counter is started at the same time as the ramp ($t = 0$), and is stopped [1] when the comparator fires ($V_i = V_r(t)$), completing the digitization. The new circuitry simply changes the start of the counter from $t = 0$ to $t = t_P$, the time at which a channel at pedestal would fire. The time t_P is determined by a "democratic election" in which every channel casts one vote, as follows. The comparator output from each channel is capacitively coupled to a common capacitor to ground in parallel with the input of a discriminator, the output of which is used to start the counter. After a certain number of comparators have fired, the voltage across the common capacitance will reach the discriminator threshold, at which point the counter will start ($t = t_P$). Because channels at pedestal fire very close in time, t_P is sharply determined. The discriminator threshold

[1] The counter (which is common to all channels) is not actually stopped, but the counter value at this time is latched into a register (one register per channel).

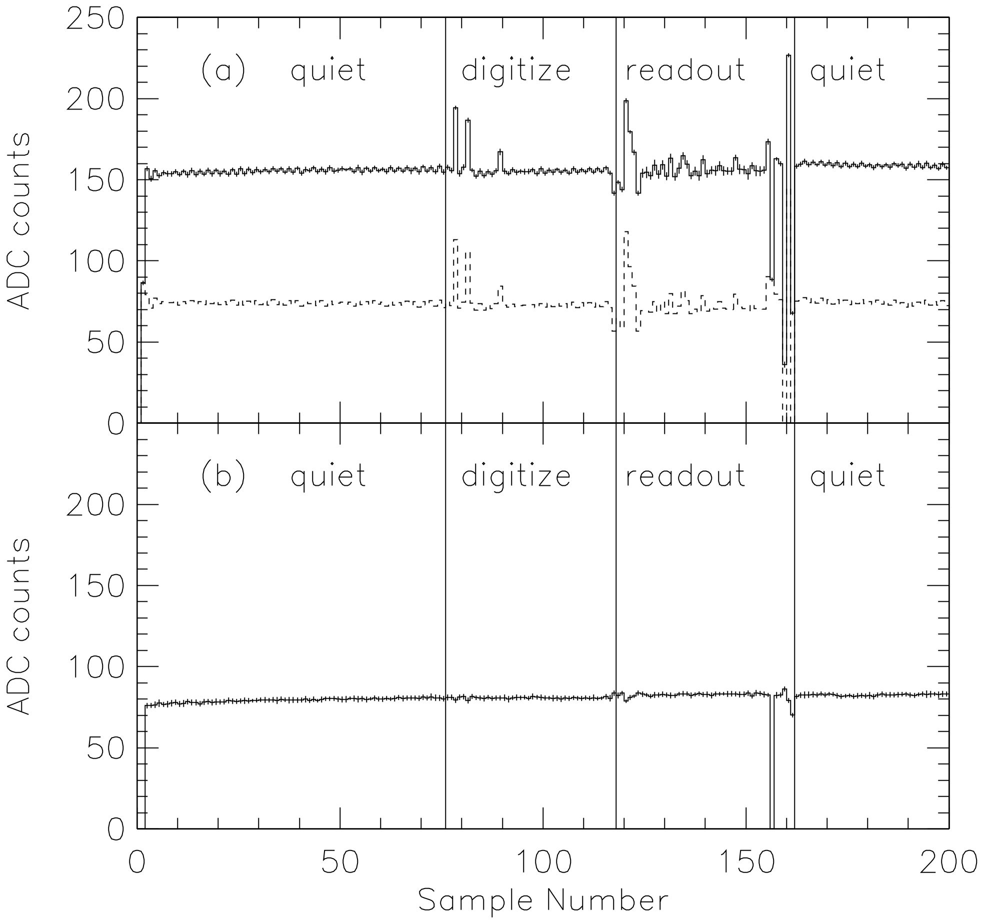

Fig. 4. Pedestal maps for SVX3D channels connected to silicon sensor strips with normal analog to digital conversion (a), and real-time pedestal subtraction (b). The solid line with error bars is for a channel to which a laser pulse was applied in every sample. The gradual rise with sample number is due to a slow variation of the laser intensity. The dashed line is for a channel without a laser pulse. Un-shielded digital signals were run over the bare sensor to introduce high environment noise. The vertical lines separate the different phases of dead-timeless operation.

is adjustable.

Since the only difference in the operation of the ADC is the point at which the counter starts, the RTPS can be enabled or disabled by a programmable register, thus allowing valuable “on vs. off” performance tests. Figure 4 (a) shows the pedestal maps for two IC channels connected to strips of a silicon sensor. RTPS is disabled. One of the strips (solid with error bars) was illuminated with an equal laser pulse during every sample, while the other one (dashed) was kept dark. High environment noise was introduced by running one side of each differential output bus line on an un-shielded wire directly over the sensor surface. Large pedestal fluctuations (common to both channels) can be seen during digitization and readout. Figure 4 (b) shows the pedestal map for the same laser-pulsed channel as (a), but now with the RTPS circuit enabled. Channels without a laser pulse cannot be seen when RTPS is enabled because pedestal is "by definition" zero ADC counts. Sample 156 (which shows zero counts) contains invalid data due to a pipeline reset operation performed at that time. For all other samples, the RTPS is seen to correctly remove the fluctuations due to environment noise.

6 Conclusion

The revision D of the SVX3 readout IC has been fabricated in a radiation hard process and shows adequate noise performance up to 4 MRad radiation dose. The IC contains several innovative features that were added in order to meet the goals of dead-timeless operation for the CDF-II detector. In particular, the low resistivity of the substrate used in the radiation hard process was exploited to achieve excellent isolation of digital and analog circuits, and a new circuit was added to the ADC that can carry out a real-time pedestal subtraction to remove common-mode noise. The SVX3D dead-timeless performance in bench tests meets specifications for construction of the silicon strip trackers of the CDF upgrade.

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References

[1] The CDF II Collaboration, CDF II Technical Design Report, FERMILAB-Pub-96/390-E (1996).

[2] T. Zimmerman *et. al.*, SVX3: A dead-timeless readout chip for silicon strip detectors, Nucl. Instr. and Meth. A 409 (1998) 369-374.

[3] M. Garcia-Sciveres, Readout electronics architecture and packaging for the CDF silicon upgrade, Nucl. Instr. and Meth. A 392 (1997) 375-379.

[4] A signal to noise ratio of better than 10 is considered necessary for track pattern recognition. The total SVX3D power consumption is 3.5 mW/channel, 30% of which is in the input transistor.

[5] S. Kleinfelder *et. al.*, A flexible 128 channel silicon strip detector instrumentation integrated circuit with sparse data readout, IEEE Trans. Nucl. Sc. NS35(1) (1988) 171.

[6] T. Zimmerman *et. al.*, The SVX2 Readout Chip, IEEE Trans. Nucl. Sc. NS42(4) (1995) 803; R. Yarema *et. al.*, A beginners guide to SVXIIE, FERMILAB-TM-1892 (1996).

[7] The n-channel dimensions are 1785.6 μm width by 1.2 μm length, and the normal operating current is 200 μA.

[8] S. Tedja *et. al.*, Noise measurement results of a radiation hardened CMOS 1.2-micrometer P well process, Nucl. Instr. and Meth. A 312 (1992) 576-584.

[9] D. Sjögren, Effects of ionizing radiation on the SVX3 chip, TRYTA-FYS-9022, Royal Institute of Technology, Stockholm, Sweden (1998).

[10] D. Fleetwood, A first principles approach to total-dose hardness assurance, IEEE NERSC '95 Short Course, Madison, WI, USA (1995).

[11] O. B. Milgrome *et. al.*, A dynamic thresholding technique for suppressing common mode noise in dead-timeless silicon strip detectors, Contributed paper to 6th International Conference on Advanced Technology and Particle Physics, Como, Italy, 5-9 October 1998.

[12] C. Tollnert, Testing of readout electronics for the silicon vertex tracker of CDF, TRITA-FYS-9026, Royal Institute of Technology, Stockholm, Sweden (1998).