Hybrid 2l30 Traveler

May 11, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 2L30 has die: 186-074 186-075

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 2l30 classification info. Created 08:53:17 05/10/00

Hybrid 2l30 quality: bad
Chip classification: bad good
Bad channels (chip-channel): 0-118 0-119 0-120 0-121
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-0-121 0-1-121 0-14-121
   0-15-121 0-21-121 0-23-121 0-24-121 0-3-121 0-35-121 0-39-121 0-4-121
   0-42-121 0-6-121 0-8-121
Channels at pedestal needed for DCMS: 28.7 30.6
```

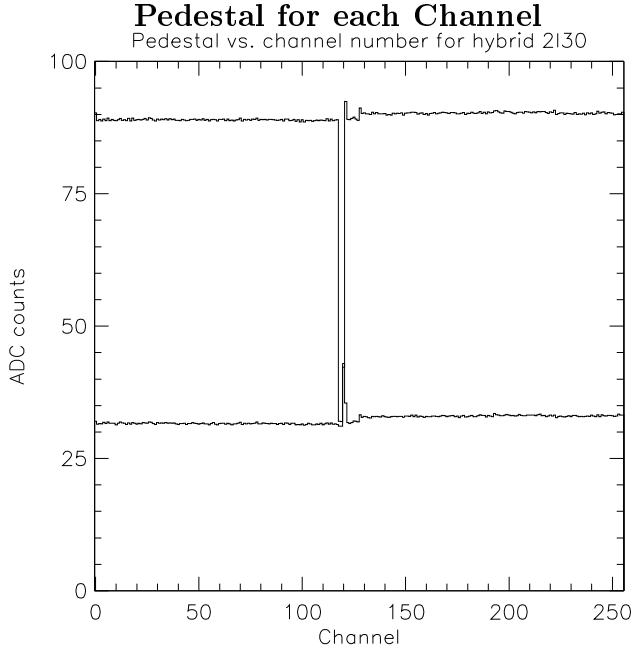
4 Comments

HV tested.

5 Pedestal

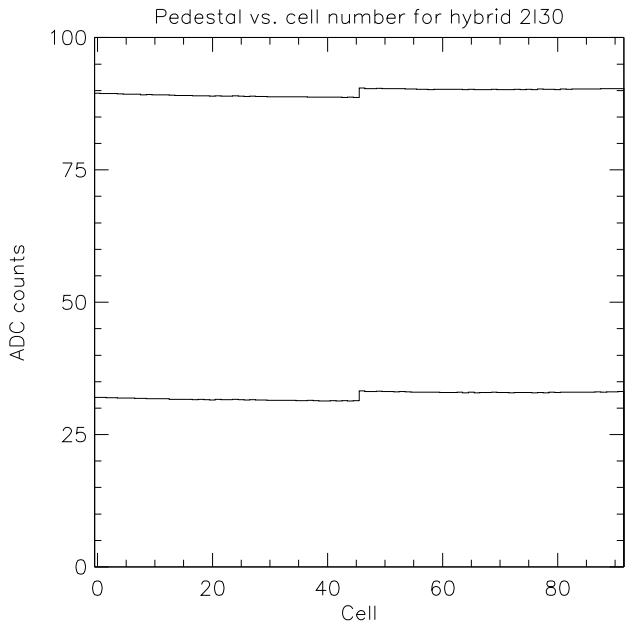
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

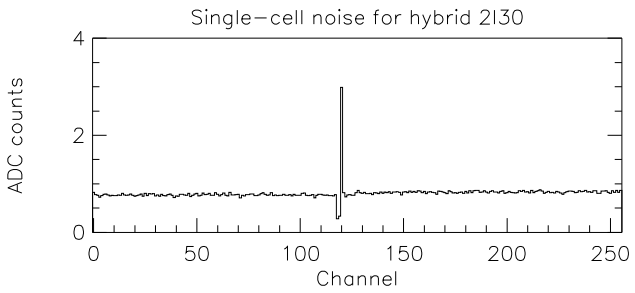
Pedestal vs. Pipeline Cell ID

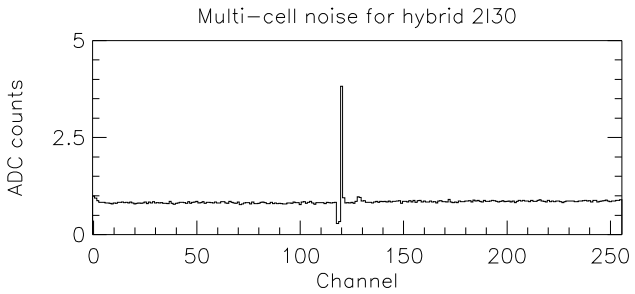


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

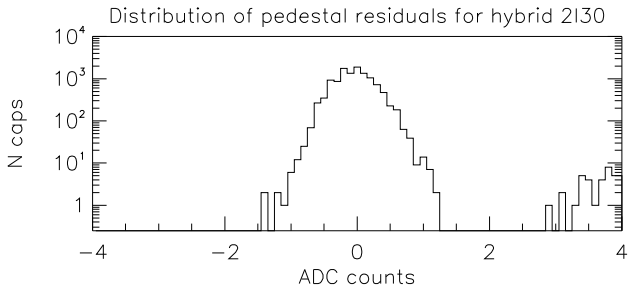
RMS Noise

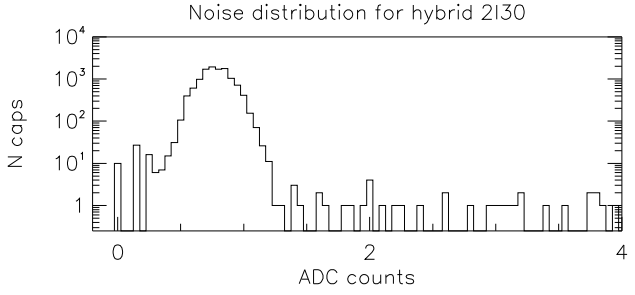




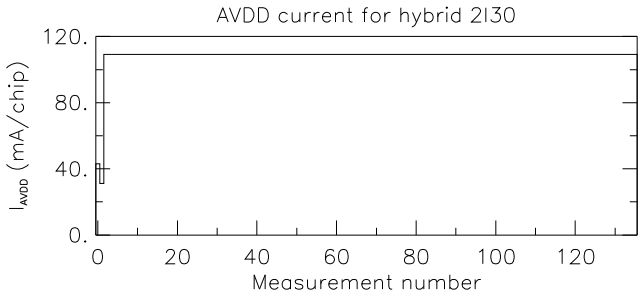
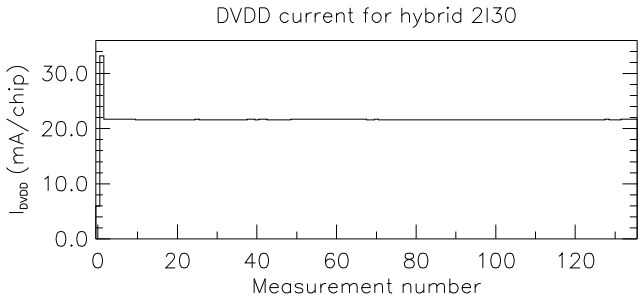
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in