# Hybrid 3p115 Traveler

December 14, 1999

## 1 Connectivity

Repairs on shorts:

Fixes for opens:

## 2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 3P115 has die: 202-047 202-049 202-050

## 3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 3p115 classification info. Created 14:48:44 12/13/99

Hybrid 3p115 quality: fair
Chip classification: fair fair fair
Bad channels (chip-channel): 0-1 1-100 2-39
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-27-40
Channels at pedestal needed for DCMS: 30.6 32.7 32.7
```

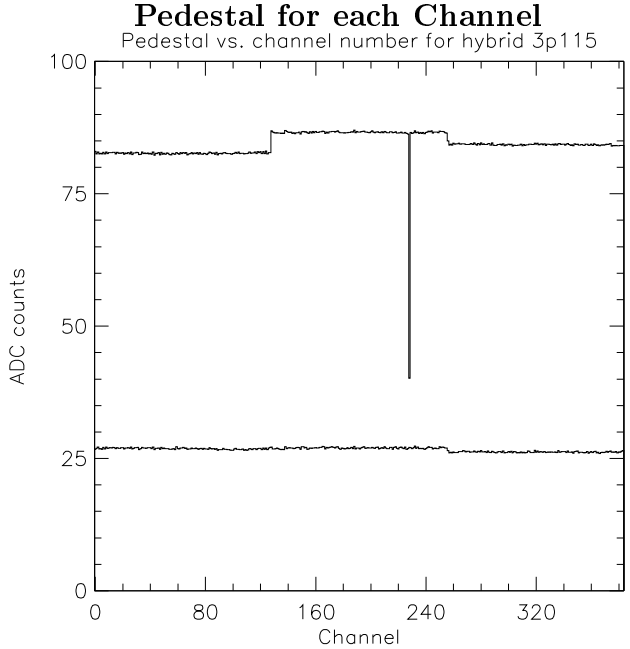
## 4 Comments

Has encasulation.
Has Au finger bonds for FE DVDD and DGND.
HV Test.

# 5 Pedestal

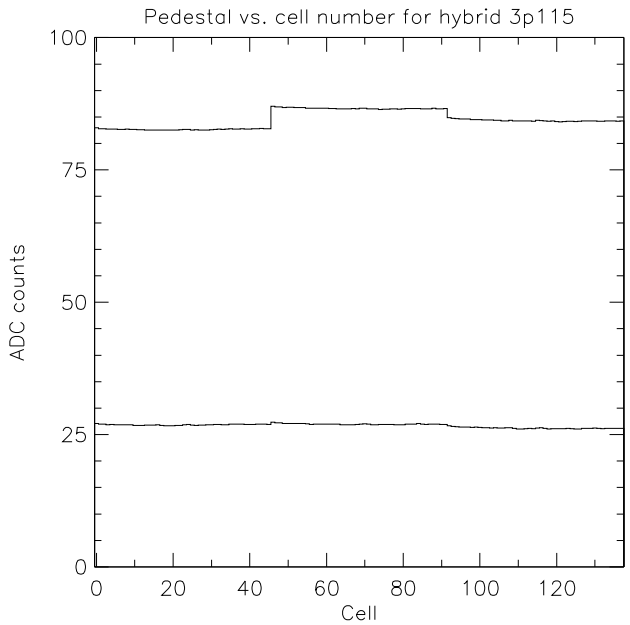
The following plot shows the pedestals vs. channel number with and without charge injection:

**Pedestal for each Channel**




The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

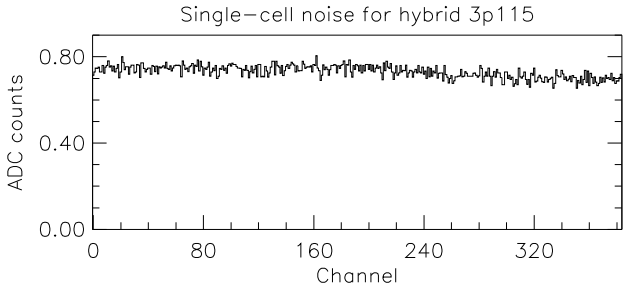
**Pedestal vs. Pipeline Cell ID**

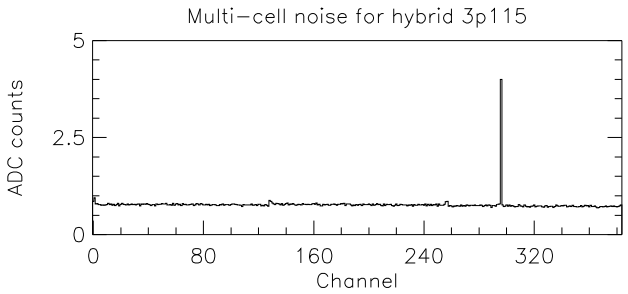


# 6 Noise

The following plots show the single-cell and multi-cell RMS noise:

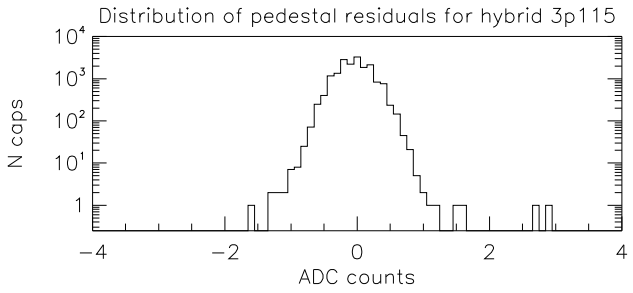
**RMS Noise**

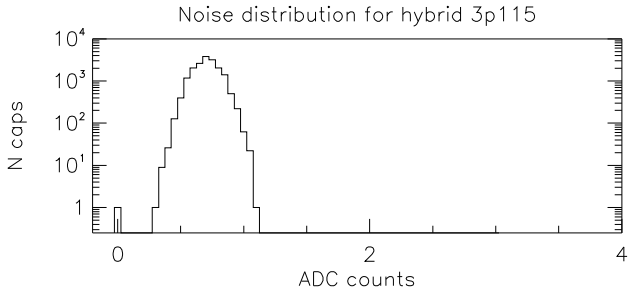


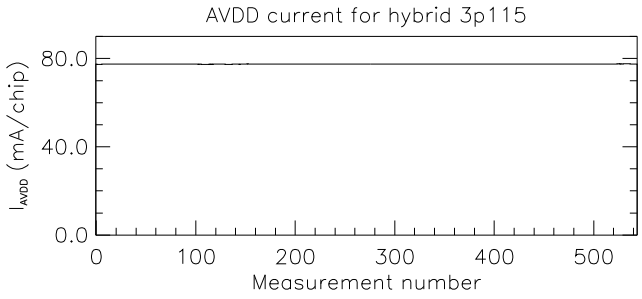
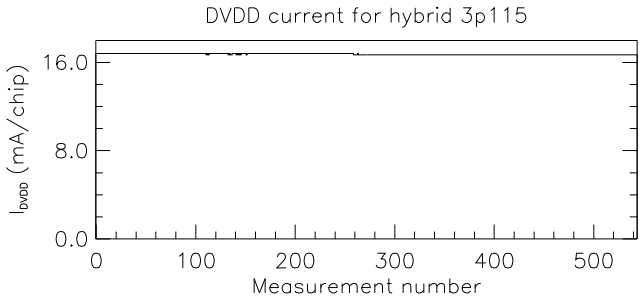

The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

**Distribution of Pedestals and Noise**



# 7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

**Supply Currents During Burn-in**