Hybrid 3p72 Traveler

January 14, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 3P72 has die: 205-122 202-010 202-013

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 3p72 classification info. Created 16:53:22 01/07/00

Hybrid 3p72 quality: fair
Chip classification: fair fair good
Bad channels (chip-channel): 1-48
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-17-25 0-17-26 0-18-25
Channels at pedestal needed for DCMS: 33.7 29.6 32.7
```

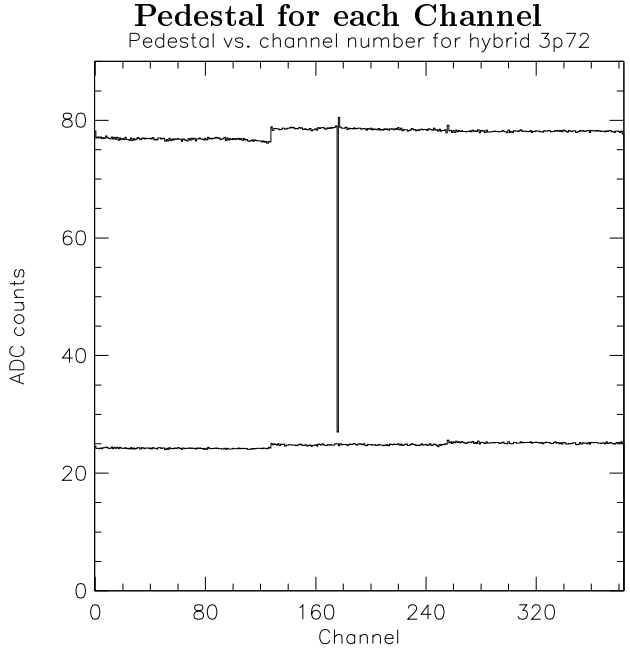
4 Comments

Chip 1 replaced.
Has Au FE DVDD and DGND wirebonds.
HV test.

5 Pedestal

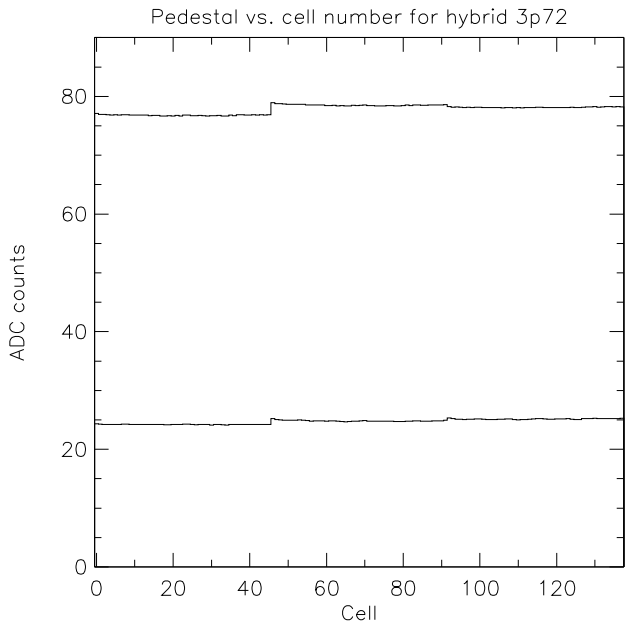
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

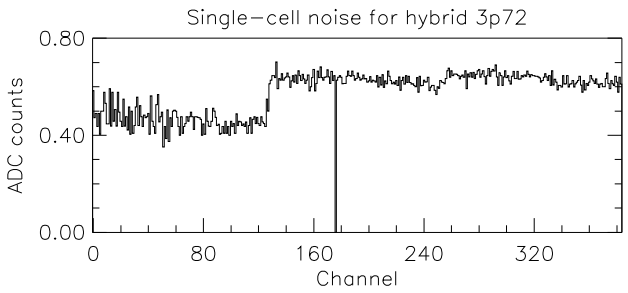
Pedestal vs. Pipeline Cell ID

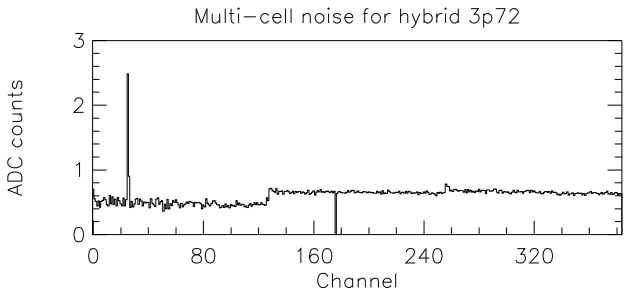


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

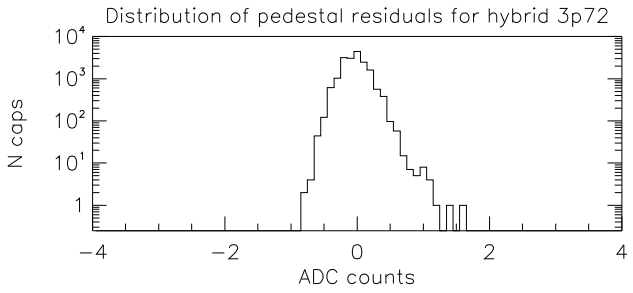
RMS Noise

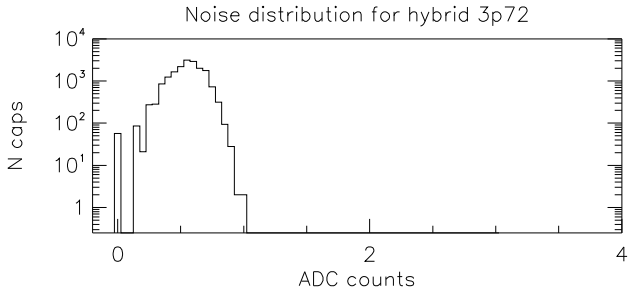




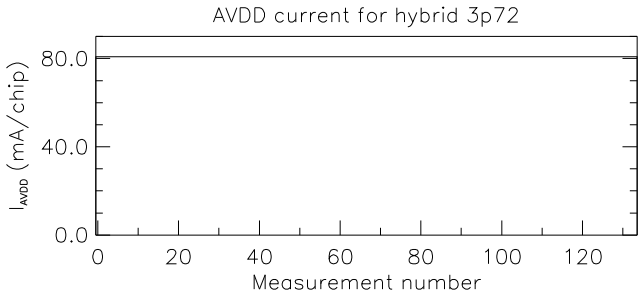
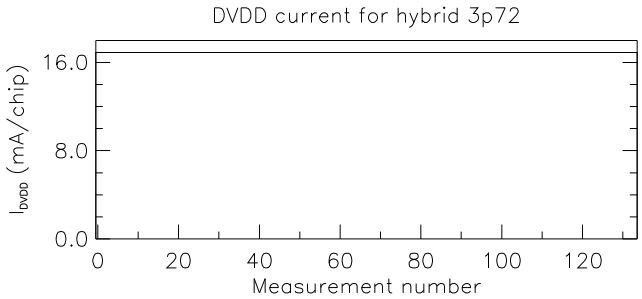
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in