Hybrid 3z65 Traveler

April 24, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:GND for Islope resistor on chip 1 open, fixed with red wire. HV open to leftmost finger: fixed with jumper.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 3Z65 has die: 196-099 196-102 196-103

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 3z65 classification info. Created 09:31:50 04/17/00

Hybrid 3z65 quality: fair
Chip classification: fair fair good
Bad channels (chip-channel): 0-3 1-49
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-20-49 1-34-49 1-37-49
   1-38-49 1-40-48 1-40-49 1-42-48 1-42-49 1-44-48 1-44-49 1-7-48
   1-7-49 1-8-49
Channels at pedestal needed for DCMS: 29.7 27.7 32.7
```

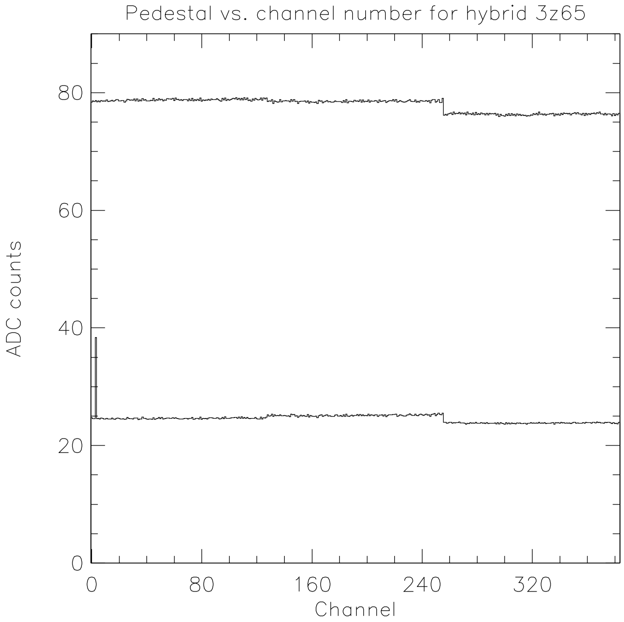
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested. Chips 1 and 2 replaced.

5 Pedestal

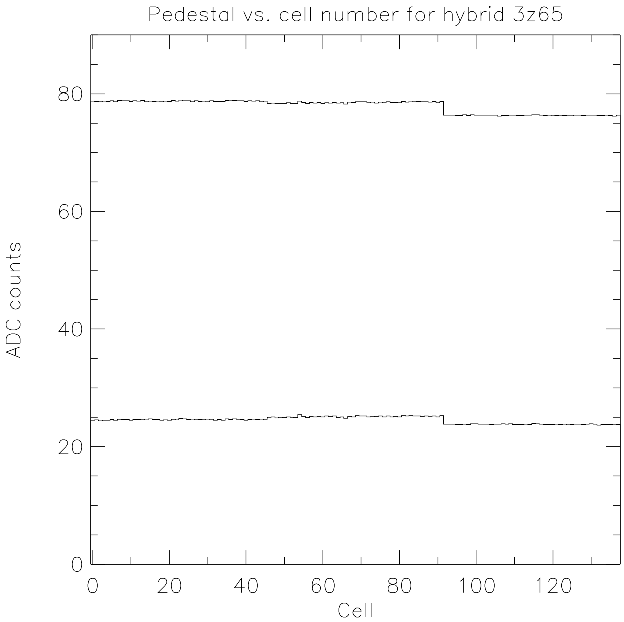
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

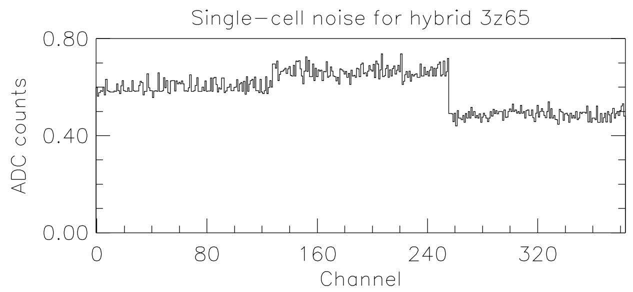
Pedestal vs. Pipeline Cell ID

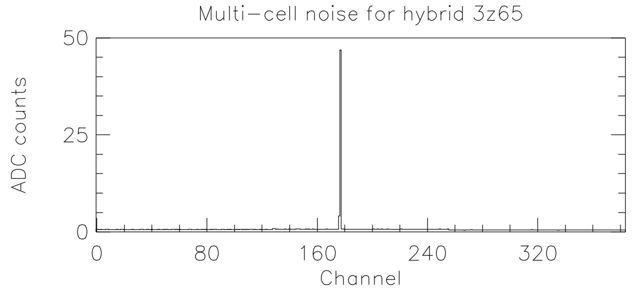


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

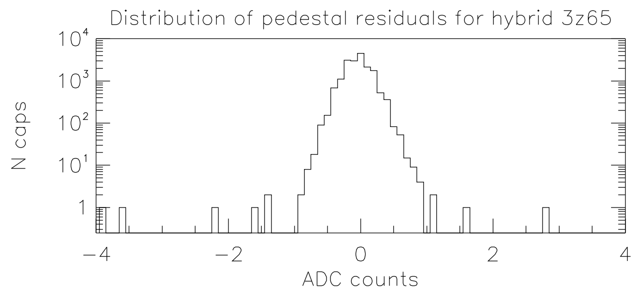
RMS Noise

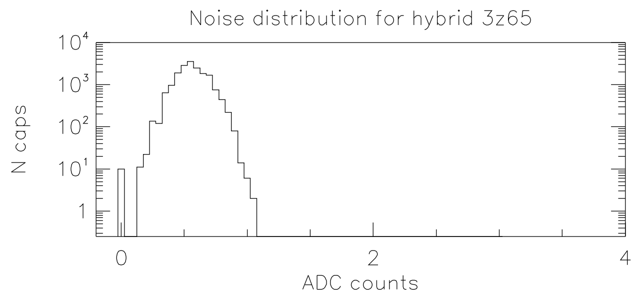




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in