Hybrid 4z110 Traveler

January 18, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: DV* open on chip 4- wirebond jumped to chip 3.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 4Z110 has die: 201-015 201-016 201-018 201-020

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 4z110 classification info. Created 16:11:31 01/17/00

Hybrid 4z110 quality: fair
Chip classification: fair fair good good
Bad channels (chip-channel): 0-10
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-1-11 0-24-86 0-24-87
   1-19-97
Channels at pedestal needed for DCMS: 27.8 28.6 25.6 27.6
```

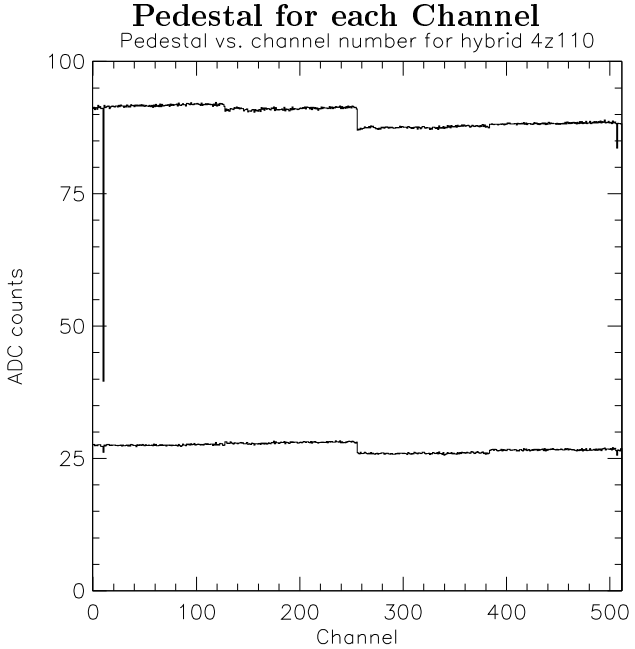
4 Comments

HV test. Has AU FE DVDD and DGND bond.

5 Pedestal

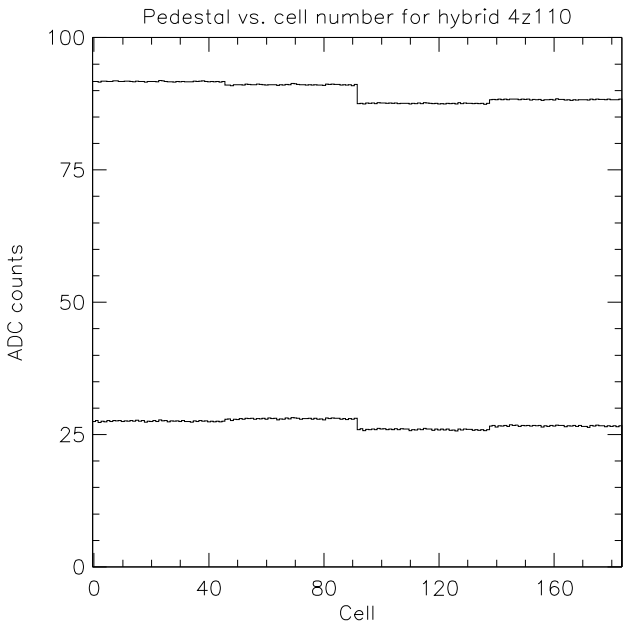
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

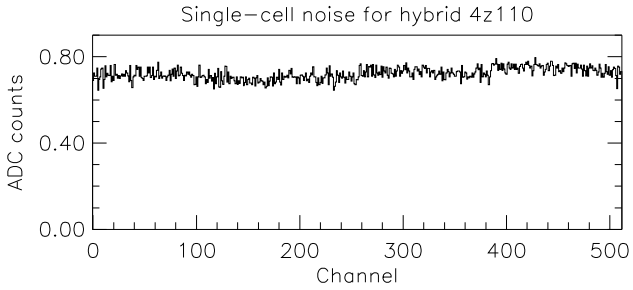
Pedestal vs. Pipeline Cell ID

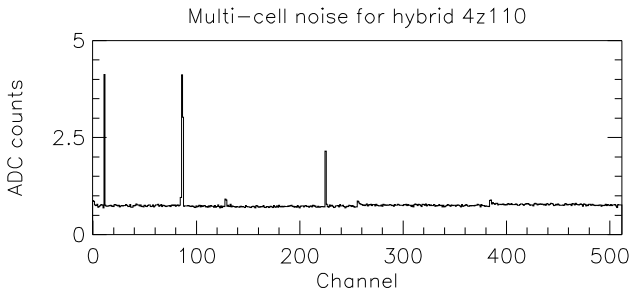


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

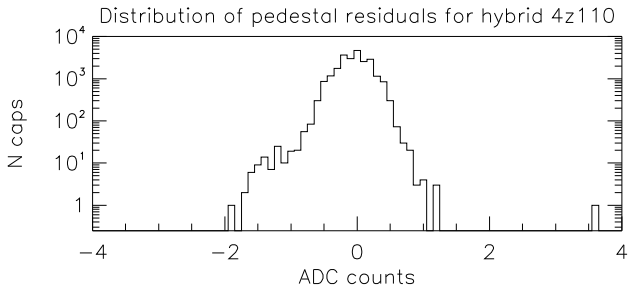
RMS Noise

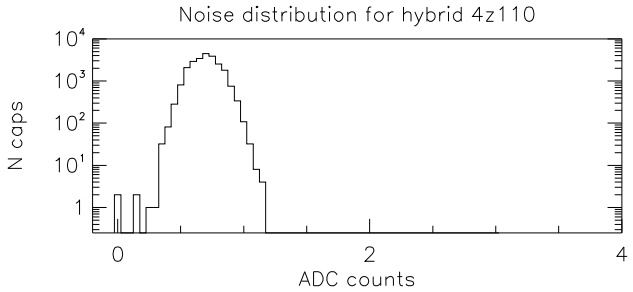




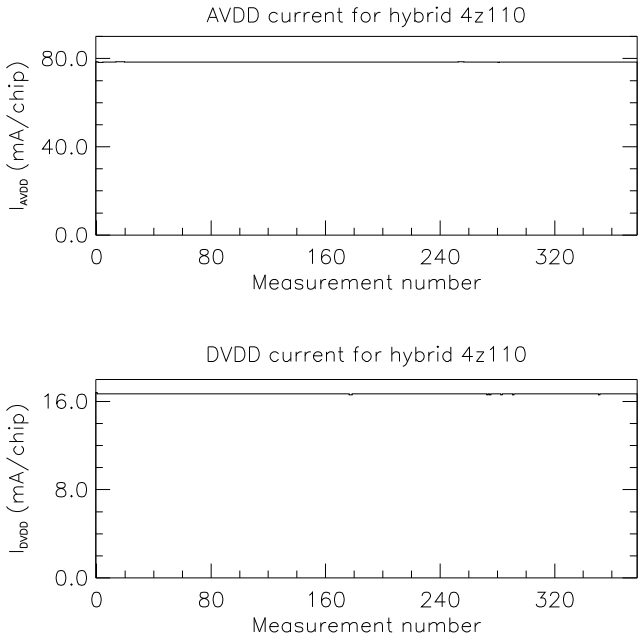
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in