Hybrid 4z126 Traveler

February 3, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: Wire bond added between chips 2, 3, and 4 for bus 1. Broken chip trace for Bus2 on Chip 3, fixed w/ wirebond.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 4Z126 has die: 201-115 201-116 201-117 201-120

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 4z126 classification info. Created 17:02:22 01/07/00

Hybrid 4z126 quality: fair
Chip classification: good fair good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-15-106 1-15-107 1-2-106
   1-2-107 1-28-106 1-28-107 1-3-107 1-32-107 1-33-107 1-35-106 1-35-107
   1-37-106 1-37-107 1-39-106 1-39-107
Channels at pedestal needed for DCMS: 27.7 31.7 30.7 27.7
```

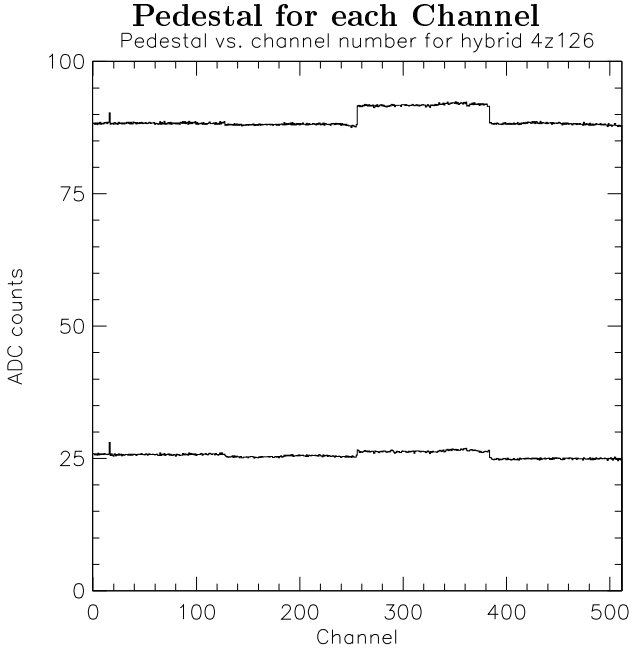
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

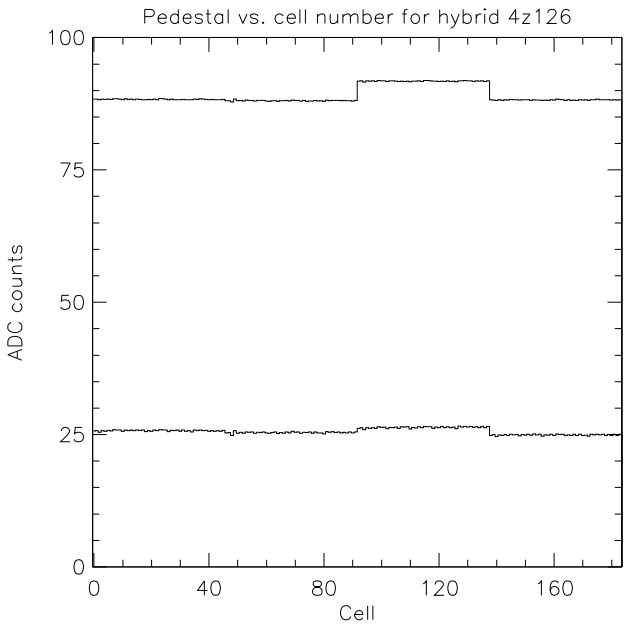
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

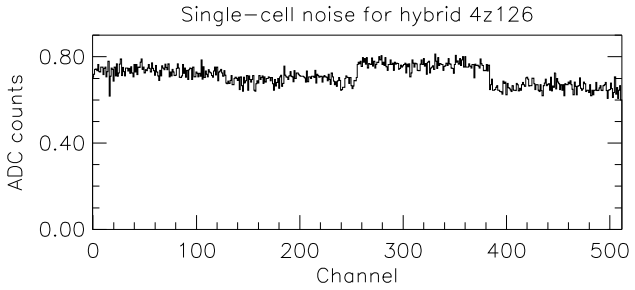
Pedestal vs. Pipeline Cell ID

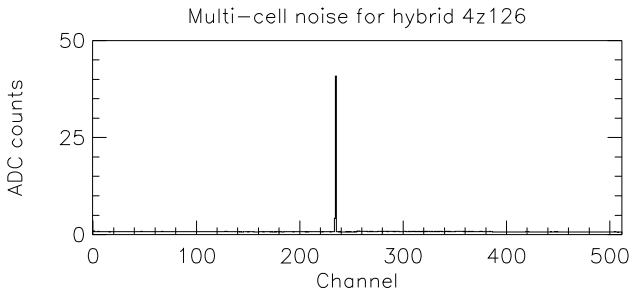


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

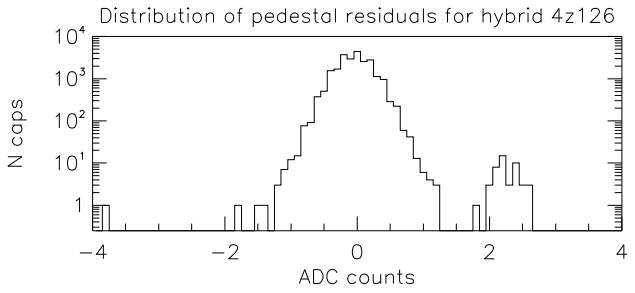
RMS Noise

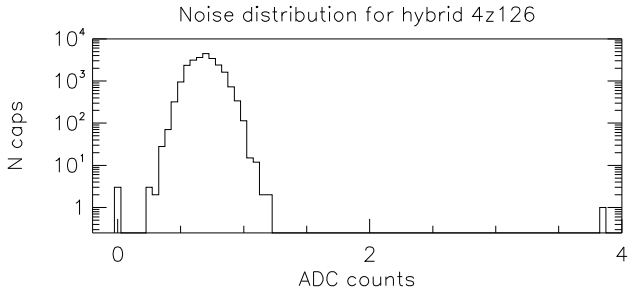




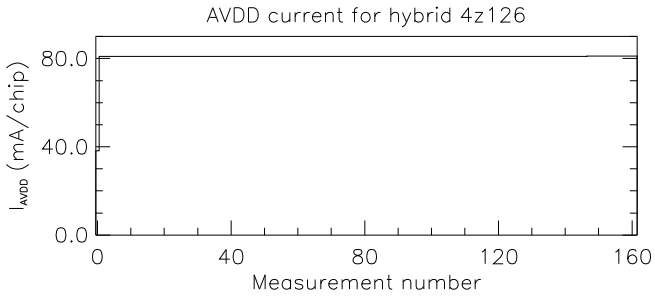
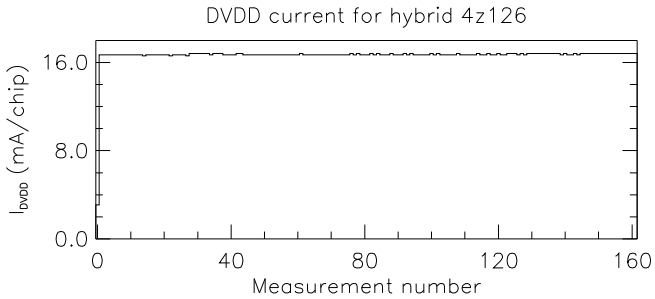
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in