Hybrid 4z202 Traveler

March 3, 2000

1 Connectivity

Repairs on shorts:
High resistance HV short to gnd in hybrid. Fixed by:

- removing 0 Ohm resistors from R5A and R5B on right side
- isolating buried HV path from right to left sides by scratching surface gold trace between the HV via (to buried HV jumper trace) and 10k Ohm resistor in R5A on left side
- adding a wire from HV+ solder pad on R5A on left side to R5A on right side

Fixes for opens:
HV trace on jumper field scratched by mistake. Fixed with small w/b.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 4Z202 has die: 160-040 160-043 160-044 160-045

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

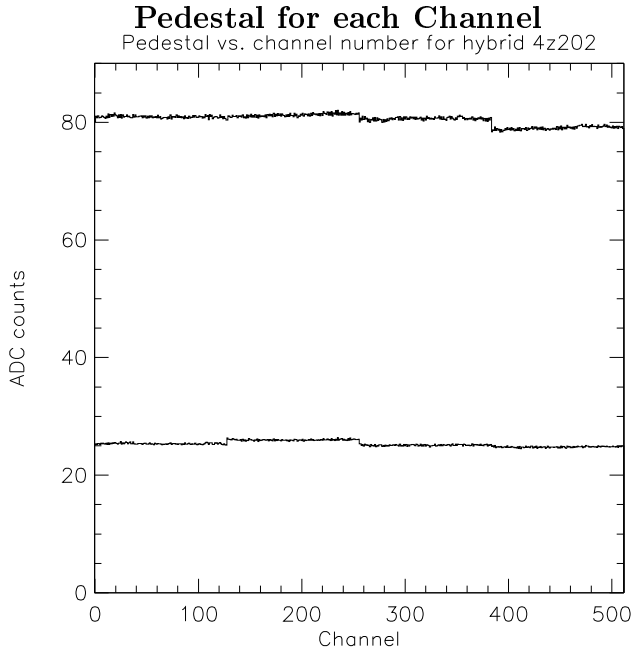
```
% Hybrid 4z202 classification info. Created 09:02:19 02/22/00

Hybrid 4z202 quality: fair
Chip classification: good fair good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-10-34 1-12-38 1-30-28
Channels at pedestal needed for DCMS: 29.7 29.6 27.8 29.6
```

4 Comments

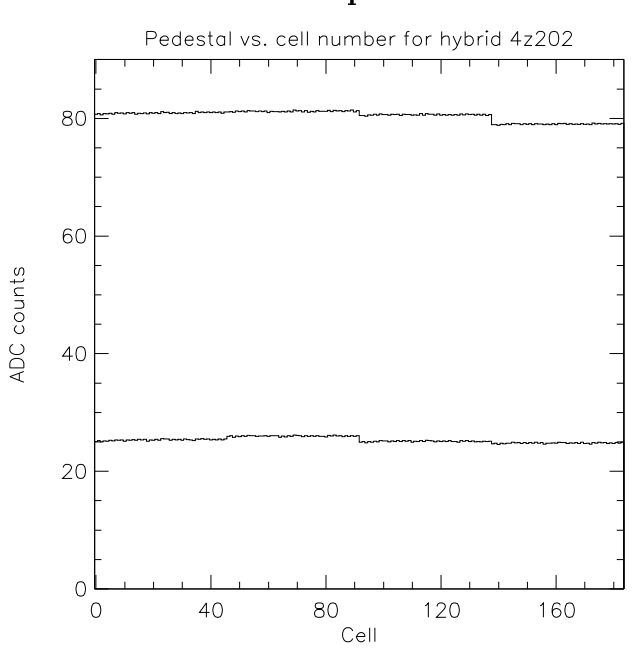
Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



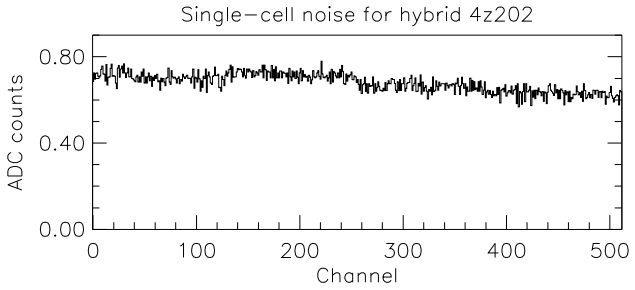
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

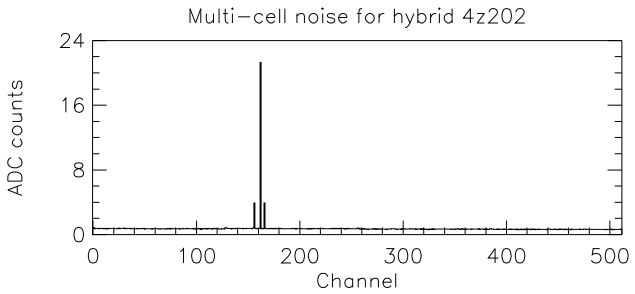


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

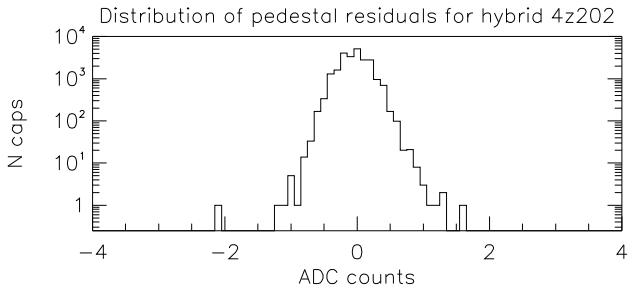
RMS Noise

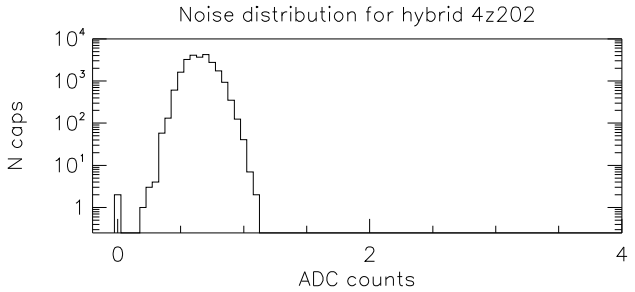




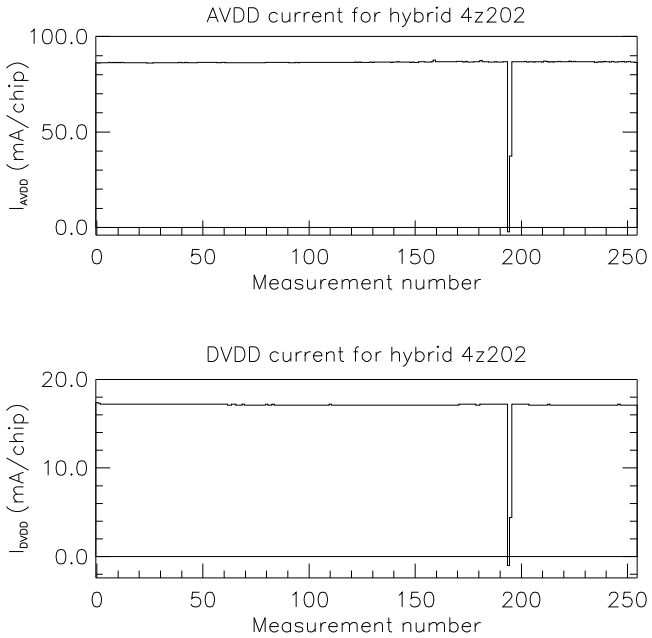
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in