Hybrid 4z55 Traveler

February 24, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 4Z55 has die: 200-104 200-106 200-107 200-108

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 4z55 classification info. Created 08:48:00 02/22/00

Hybrid 4z55 quality: fair
Chip classification: good good good fair
Bad channels (chip-channel): 3-36 3-37
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-11-36 3-13-36 3-15-36
   3-17-36 3-19-36 3-21-36 3-23-36 3-24-36 3-25-36 3-26-36 3-28-36
   3-29-36 3-30-36 3-32-36 3-34-36 3-38-36 3-39-36 3-40-36 3-42-36
   3-9-36
Channels at pedestal needed for DCMS: 30.6 30.5 25.6 26.6
```

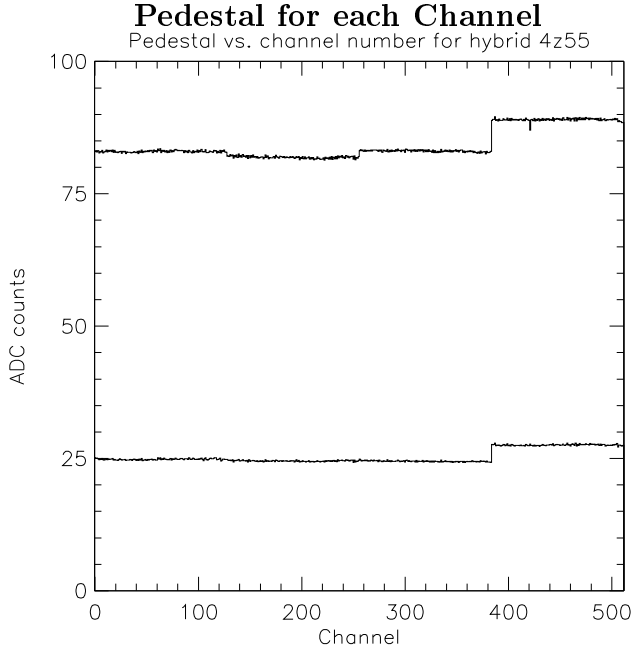
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

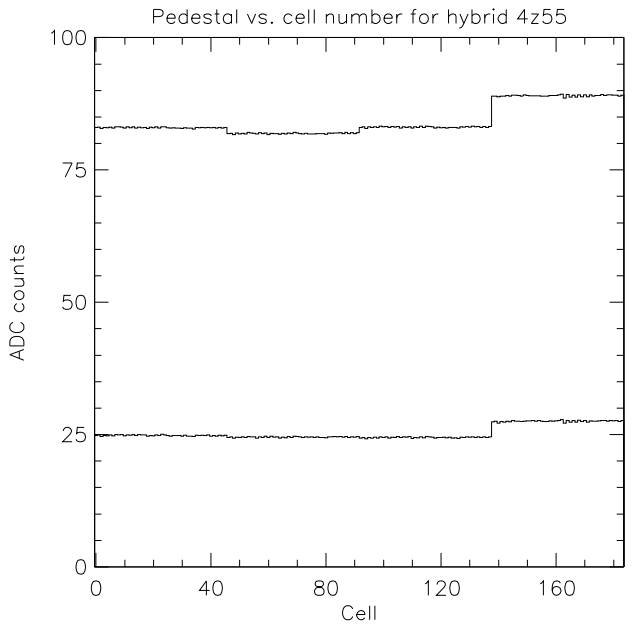
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

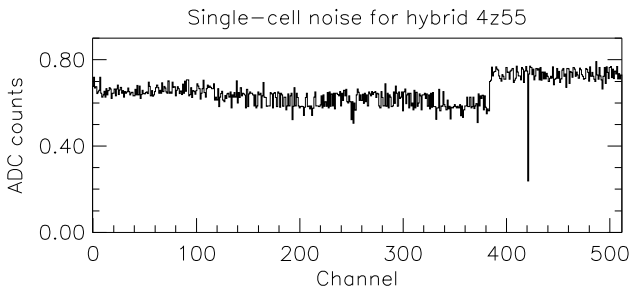
Pedestal vs. Pipeline Cell ID

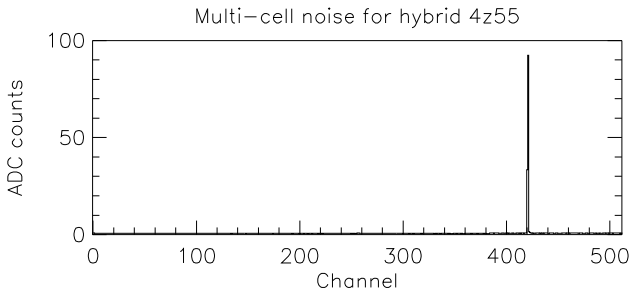


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

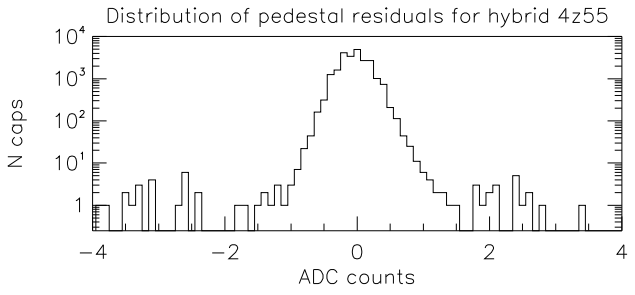
RMS Noise

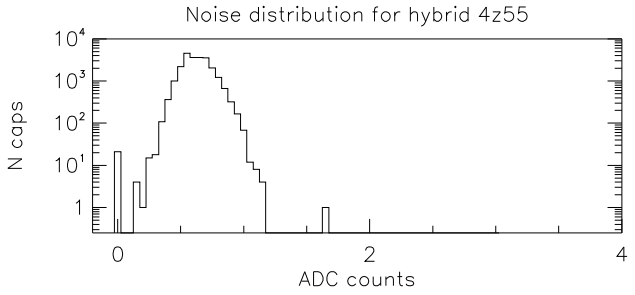




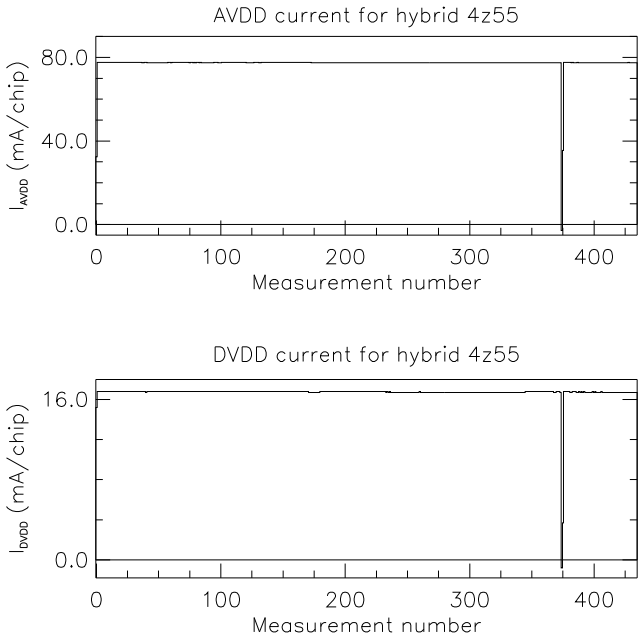
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in