Hybrid 5p102 Traveler

January 14, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P102 has die: 205-014 217-109 217-110 217-115 217-118

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5p102 classification info. Created 11:39:20 01/13/00

Hybrid 5p102 quality: fair
Chip classification: good good fair good fair
Bad channels (chip-channel): 2-67 2-120
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-1-0 2-18-50 2-20-67
   2-5-6 4-10-15 4-10-16 4-10-17 4-11-105
Channels at pedestal needed for DCMS: 33.5 37.6 35.5 35.7 38.6
```

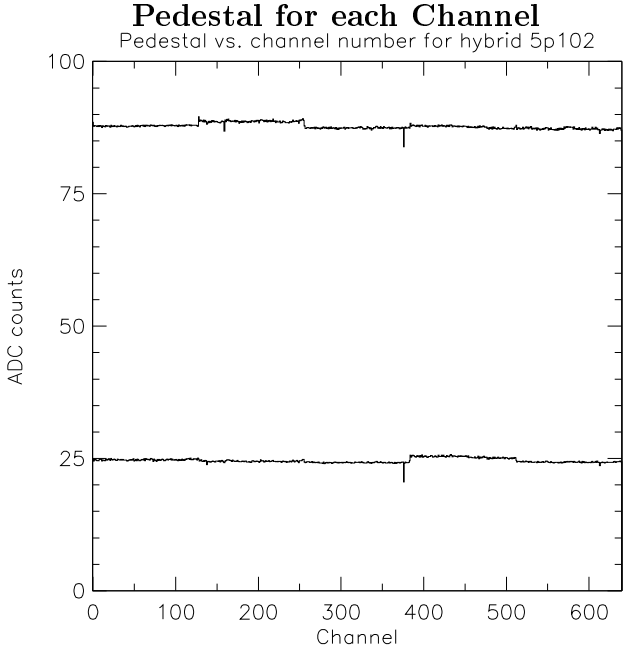
4 Comments

Has Au FE DVDD and DGND wirebonds.
HV test.

5 Pedestal

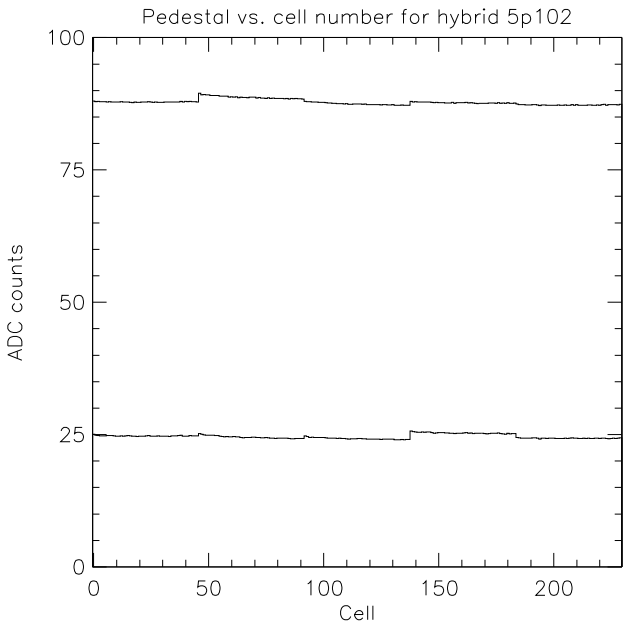
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

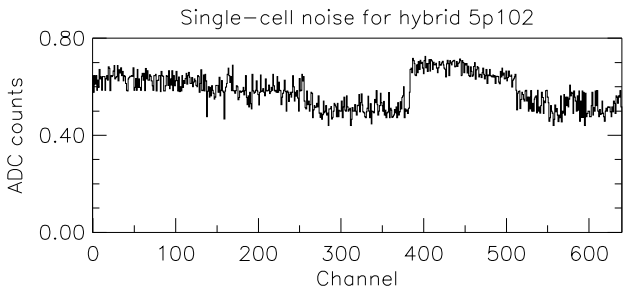
Pedestal vs. Pipeline Cell ID

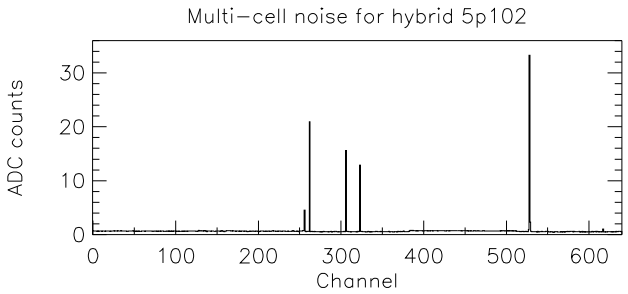


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

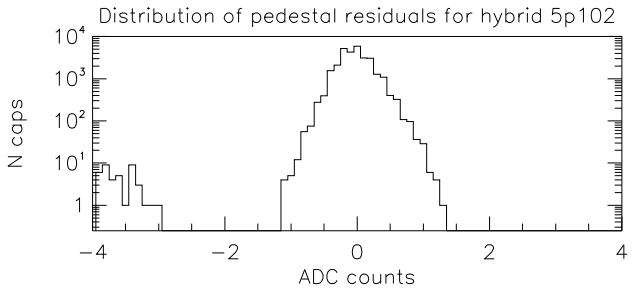
RMS Noise

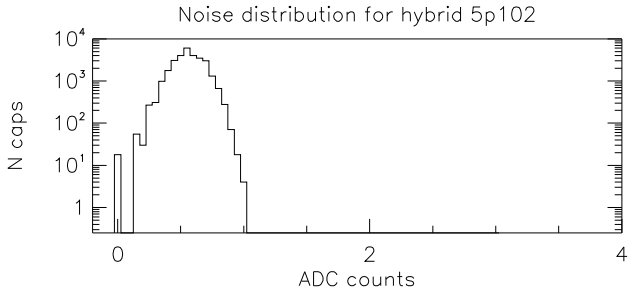




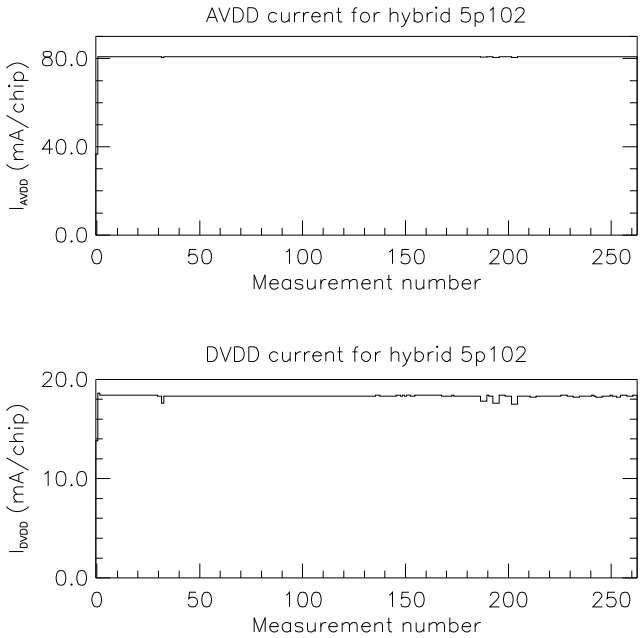
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in