Hybrid 5p104 Traveler

December 8, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P104 has die: 198-076 198-077 198-078 198-079 198-080

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

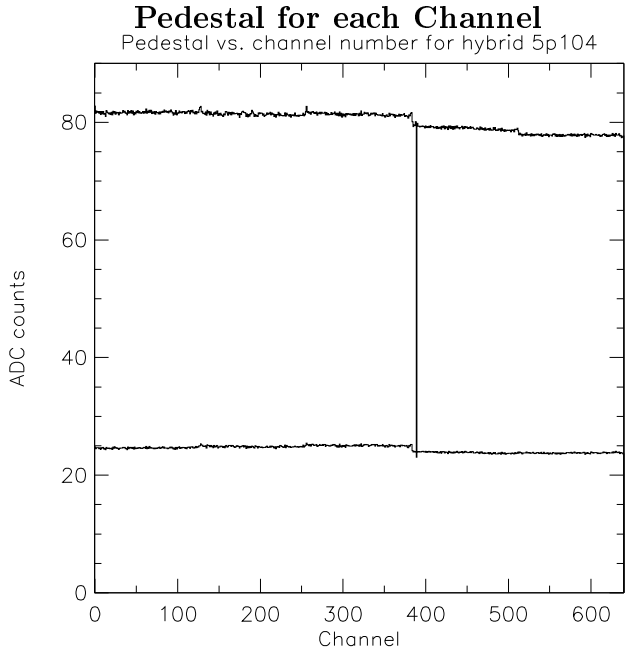
```
% Hybrid 5p104 classification info. Created 09:05:38 12/06/99

Hybrid 5p104 quality: fair
Chip classification: fair good good fair good
Bad channels (chip-channel): 3-5
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-45-0
Channels at pedestal needed for DCMS: 31.6 34.5 35.7 30.6 35.7
```

4 Comments

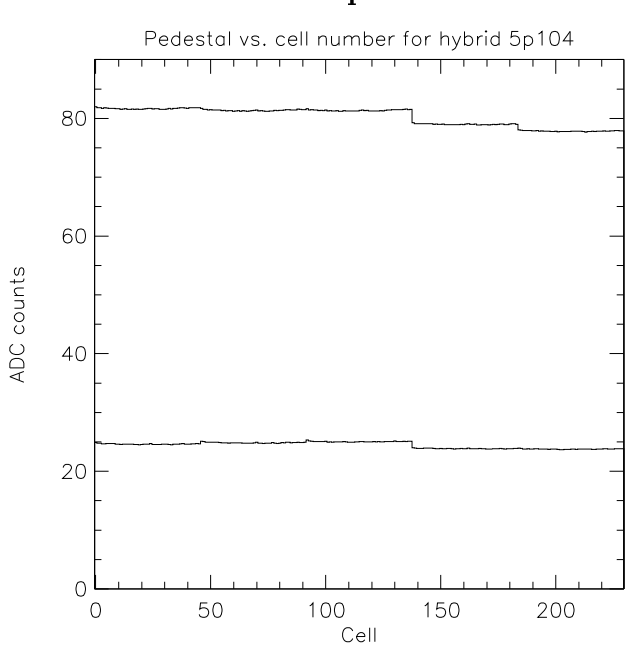
Has Au finger bonds for FE DVDD and DGND.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



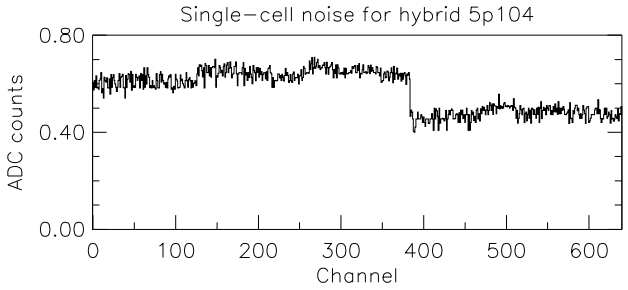
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

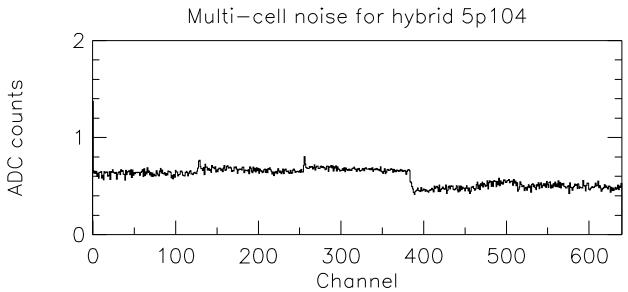


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

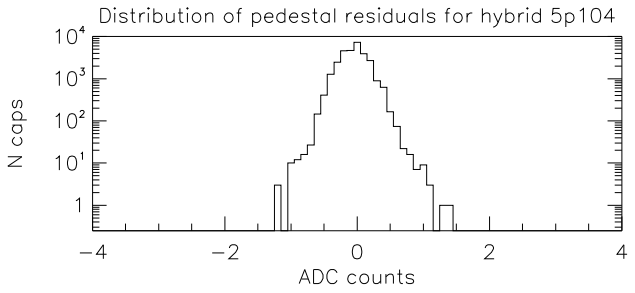
RMS Noise

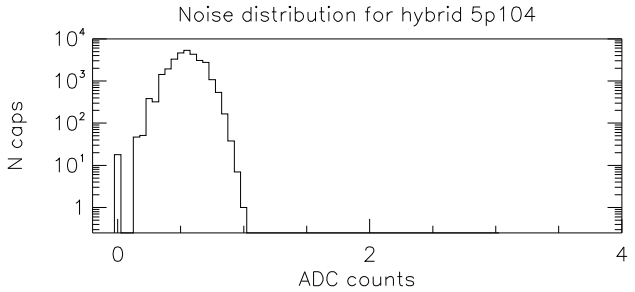




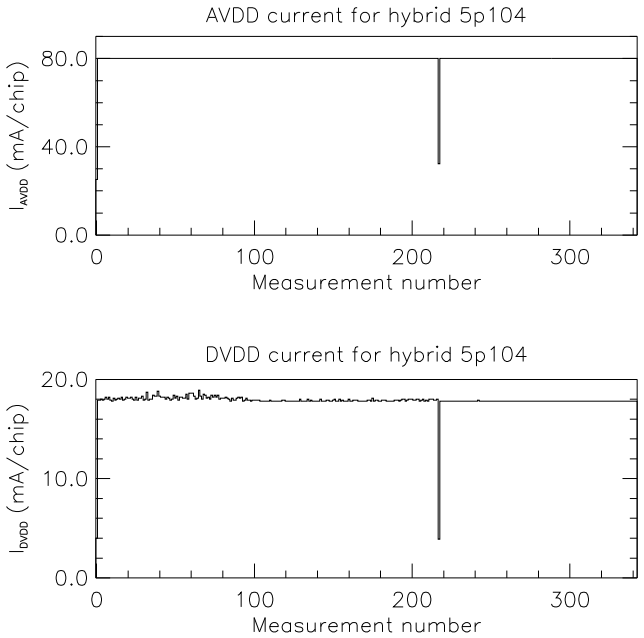
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in