Hybrid 5p160 Traveler

February 17, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: TN open between the cable and the trace to chip one. Wire added to fix. Bus 3 open to chip 4 and 5; fixed with wirebond. Bus 0 open in cable; fixed with added wire.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P160 has die: 044-010 044-011 204-007 044-013 044-017

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5p160 classification info. Created 11:48:18 01/10/00

Hybrid 5p160 quality: fair
Chip classification: good good fair good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-24-0 2-25-0
Channels at pedestal needed for DCMS: 37.6 33.7 32.6 31.6 34.3
```

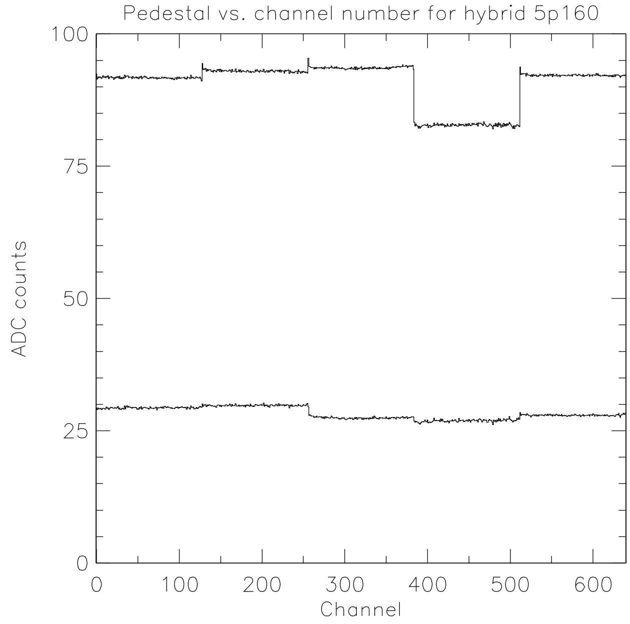
4 Comments

Chip 3 replaced. Has redundant FE DVDD, DGND bonds. HV test.

5 Pedestal

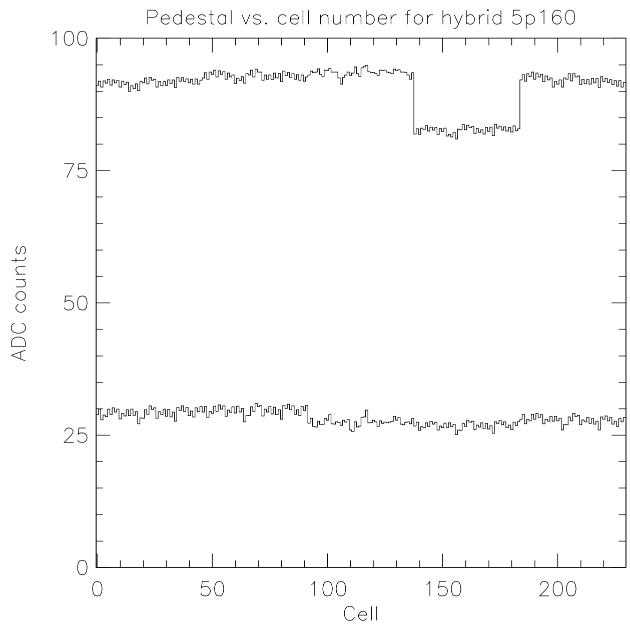
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

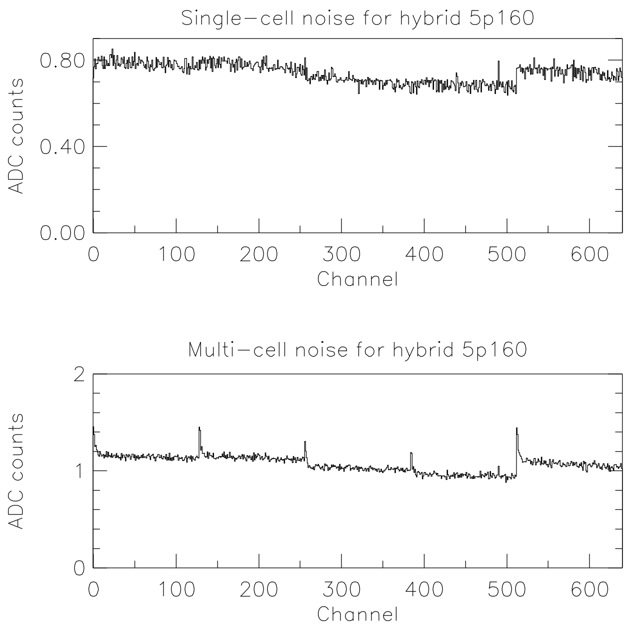
Pedestal vs. Pipeline Cell ID



6 Noise

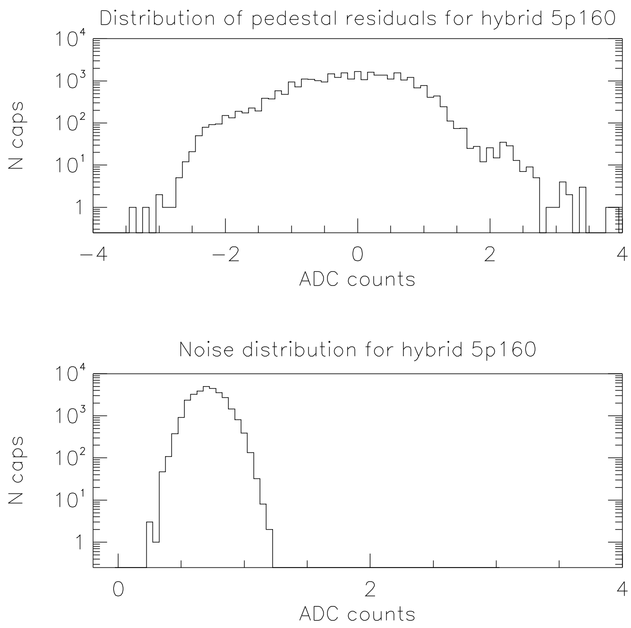
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in