# Hybrid 5p193 Traveler

May 1, 2000

## 1 Connectivity

Repairs on shorts:
Fixes for opens:

## 2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P193 has die: 158-061 158-063 158-067 158-068 158-071

## 3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5p193 classification info. Created 09:39:49 05/01/00

Hybrid 5p193 quality: fair
Chip classification: fair fair fair fair good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-37-117 0-7-116 0-7-117
   0-7-118 0-7-119 0-8-117 0-8-118 1-3-77 2-1-109 2-21-109 2-23-109
   2-25-109 2-34-108 2-34-109 2-35-109 3-29-84 3-29-85
Channels at pedestal needed for DCMS: 29.4 31.7 30.7 32.7 31.7
```

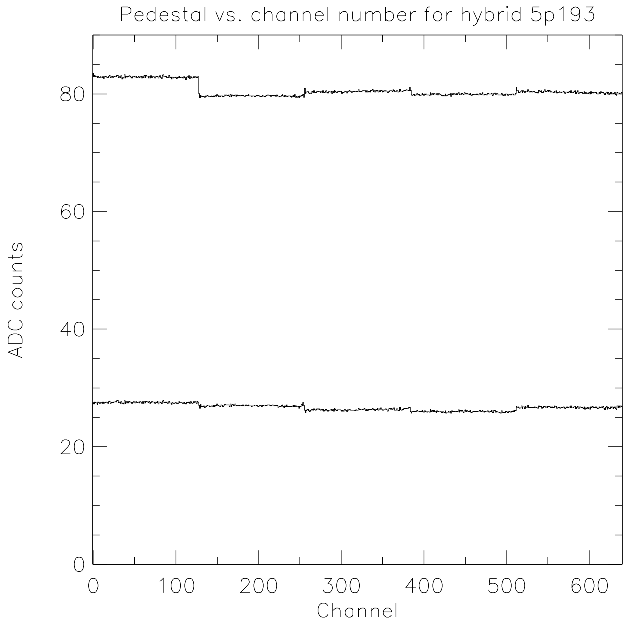
## 4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

# 5 Pedestal

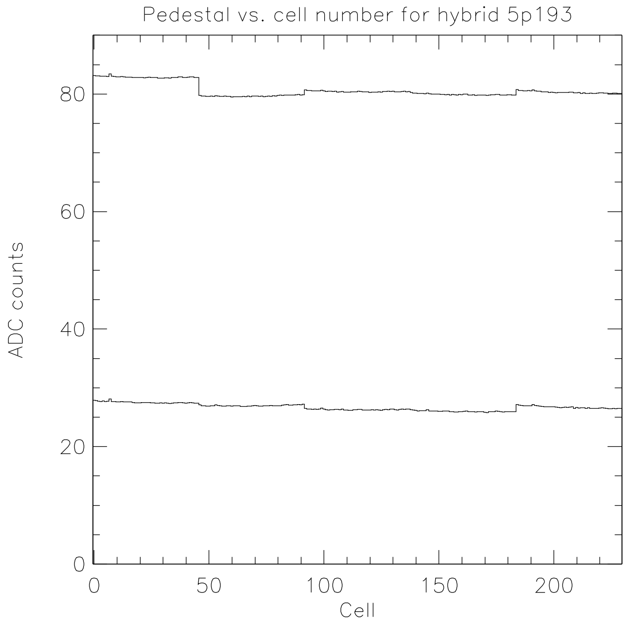
The following plot shows the pedestals vs. channel number with and without charge injection:

**Pedestal for each Channel**




The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

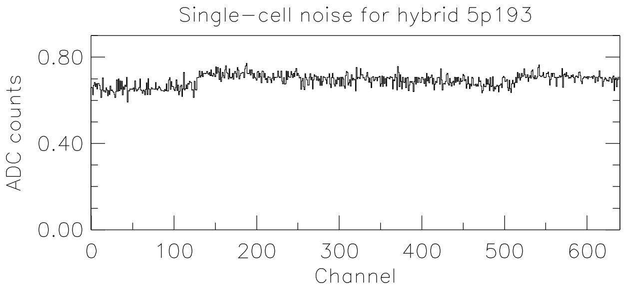
**Pedestal vs. Pipeline Cell ID**

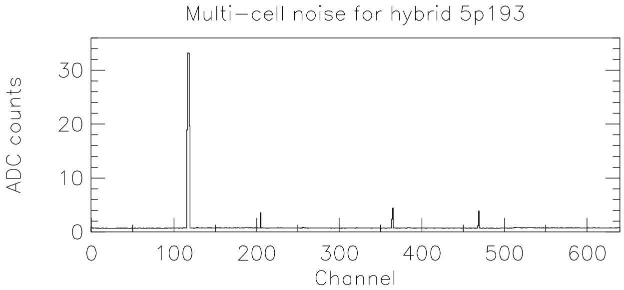


# 6 Noise

The following plots show the single-cell and multi-cell RMS noise:

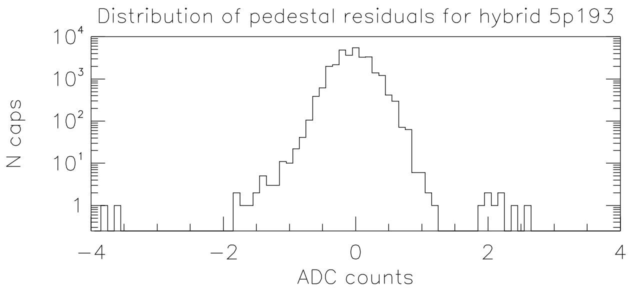
**RMS Noise**

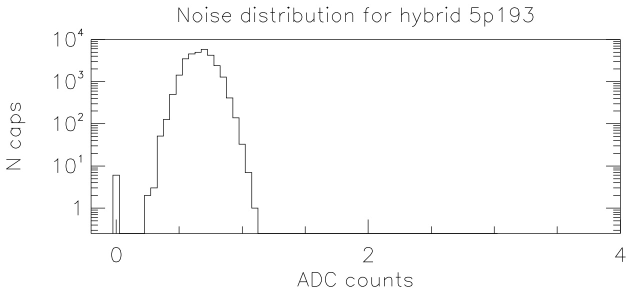



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

**Distribution of Pedestals and Noise**



# 7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

**Supply Currents During Burn-in**