Hybrid 5p48 Traveler

March 10, 2000

1 Connectivity

Repairs on shorts:
High resistance HV- short to gnd in hybrid. Fixed by:

- scratching HV- trace (under dielectric) coming from cable field to hybrid
- scratching "HV+" surface trace between HV resistor on left side and HV via at corner of trace
- adding a wire from HV- on cable field to HV resistor

Fixes for opens:
AVDD2 trace accidentally cut from cable field to solder pad. Fixed with extra wire.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P48 has die: 162-054 162-058 162-059 162-060 162-061

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5p48 classification info. Created 16:31:34 03/03/00

Hybrid 5p48 quality: fair
Chip classification: fair good good good good
Bad channels (chip-channel): 0-75
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-38-38 0-40-84
Channels at pedestal needed for DCMS: 31.6 33.1 33.6 36.6 32.6
```

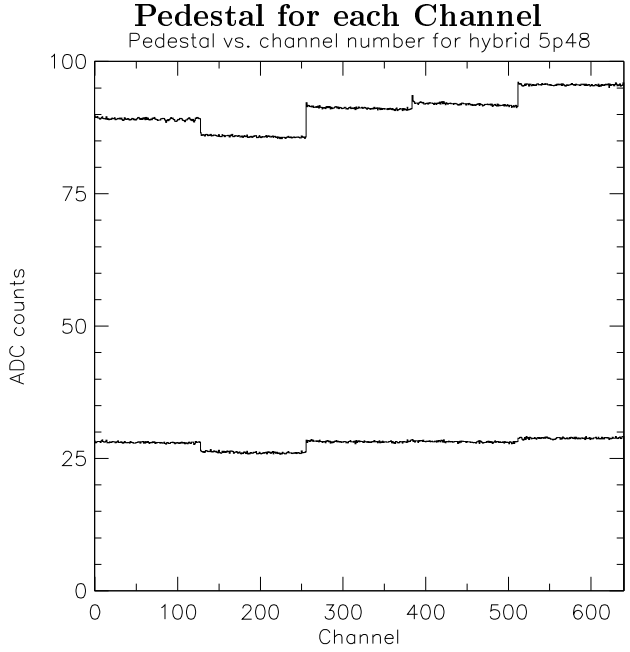
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

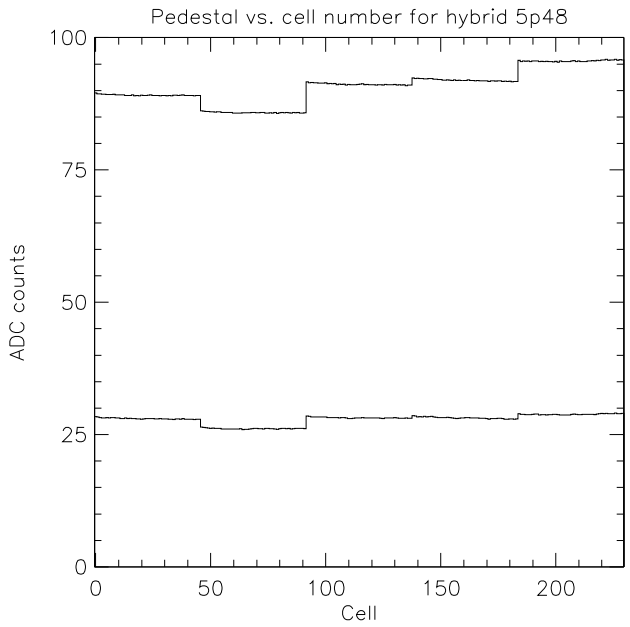
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

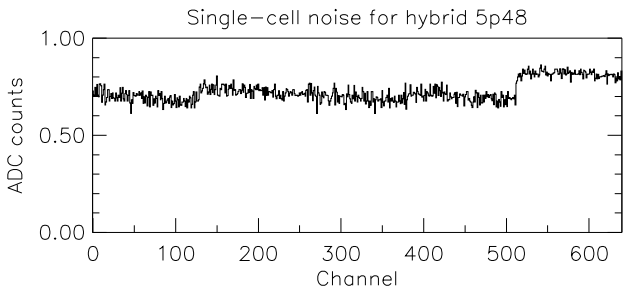
Pedestal vs. Pipeline Cell ID

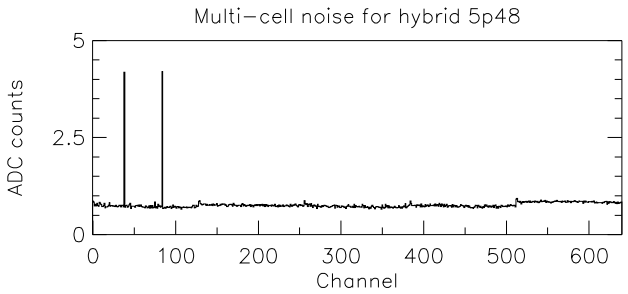


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

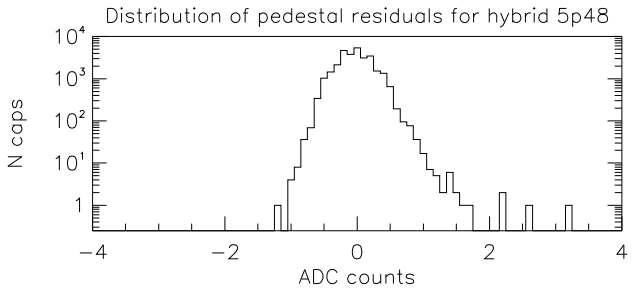
RMS Noise

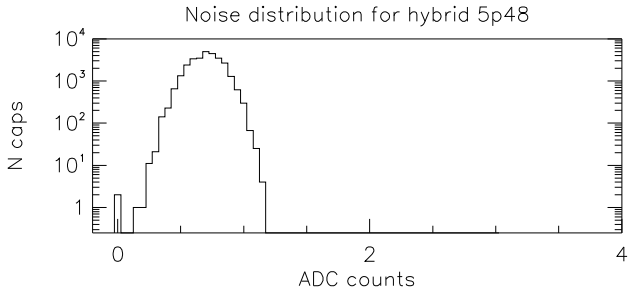




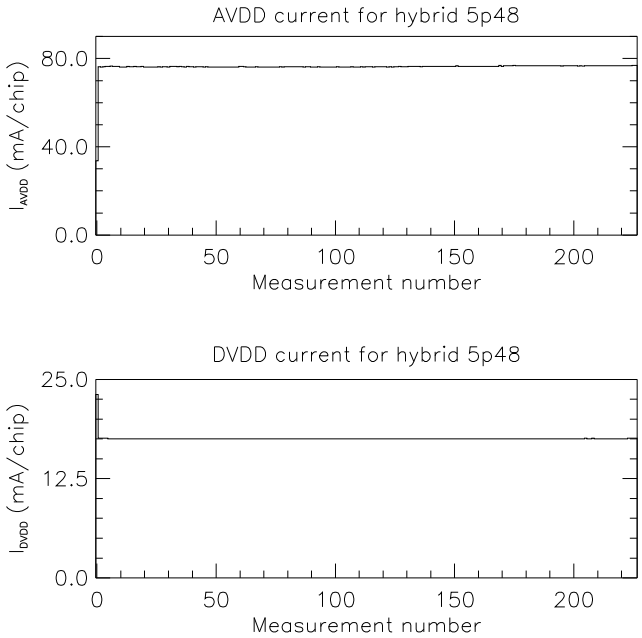
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in