Hybrid 5p68 Traveler

November 22, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P68 has die: 034-042 034-043 034-045 034-046 034-047

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5p68 classification info. Created 11:56:28 11/22/99

Hybrid 5p68 quality: fair
Chip classification: good good fair good good
Bad channels (chip-channel): 2-28
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-0-38 2-1-38 2-10-38
   2-11-38 2-12-38 2-14-38 2-15-38 2-16-38 2-18-38 2-19-38 2-2-38
   2-20-38 2-21-38 2-24-38 2-27-38 2-28-38 2-32-38 2-34-38 2-37-38
   2-38-38 2-4-38 2-5-38 2-8-38
Channels at pedestal needed for DCMS: 31.7 34.7 36.7 34.6 33.6
```

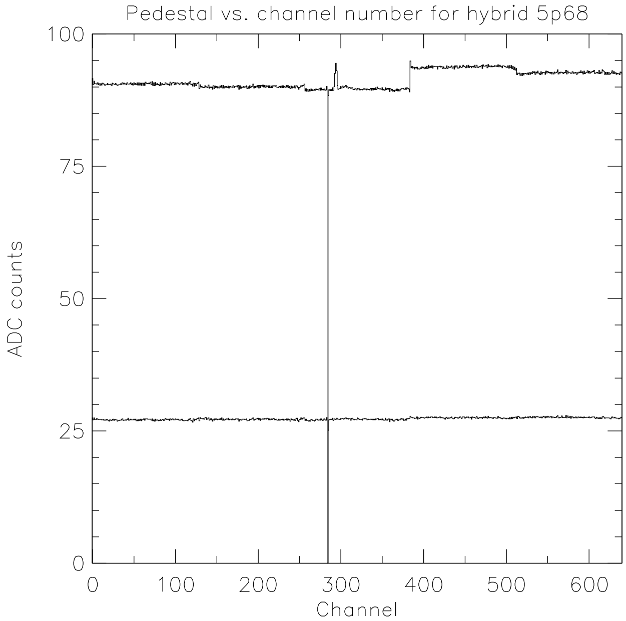
4 Comments

Automatic chip-to-chip bonds

5 Pedestal

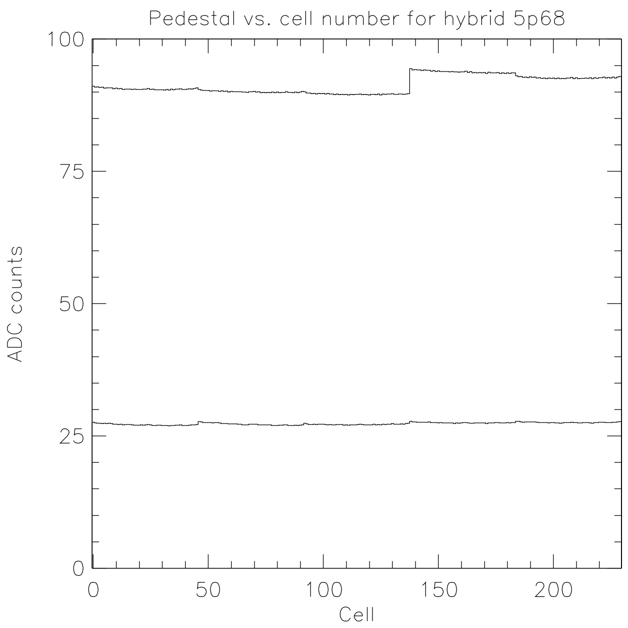
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

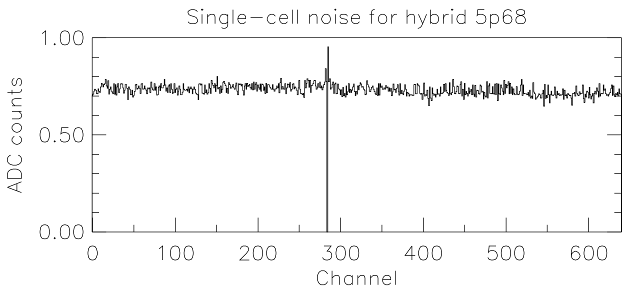
Pedestal vs. Pipeline Cell ID

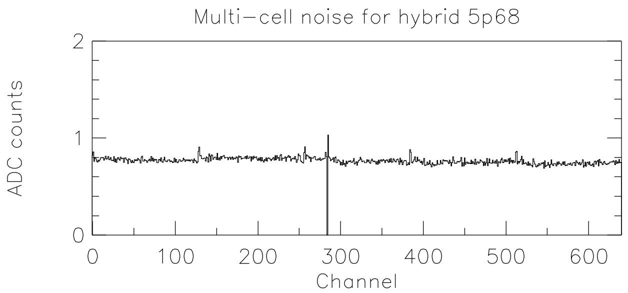


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

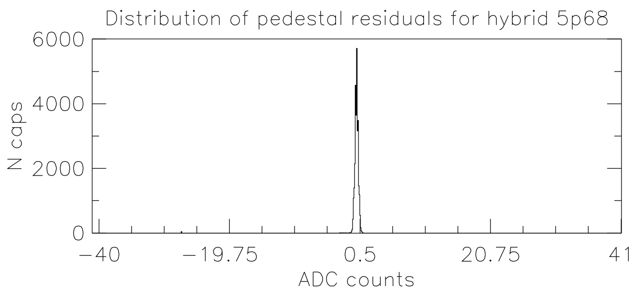
RMS Noise

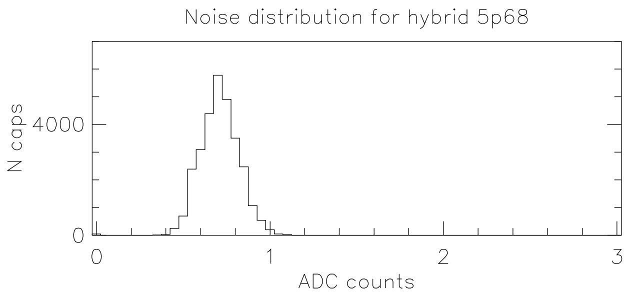




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in