Hybrid 5p72 Traveler

January 18, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5P72 has die: 195-042 195-046 195-047 195-048 195-049

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5p72 classification info. Created 17:08:45 01/14/00

Hybrid 5p72 quality: fair
Chip classification: fair good fair good fair
Bad channels (chip-channel): 0-38 0-39 2-81 2-113 4-11
Bad cells: none
Random bad capacitors: none
Channels at pedestal needed for DCMS: 28.7 33.7 33.7 36.7 32.7
```

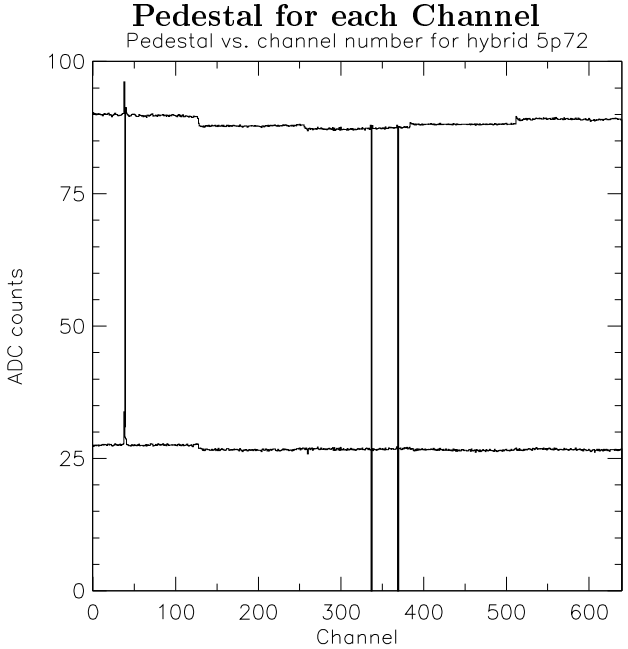
4 Comments

Has Au FE DVDD and DGND wirebonds.
HV test.

5 Pedestal

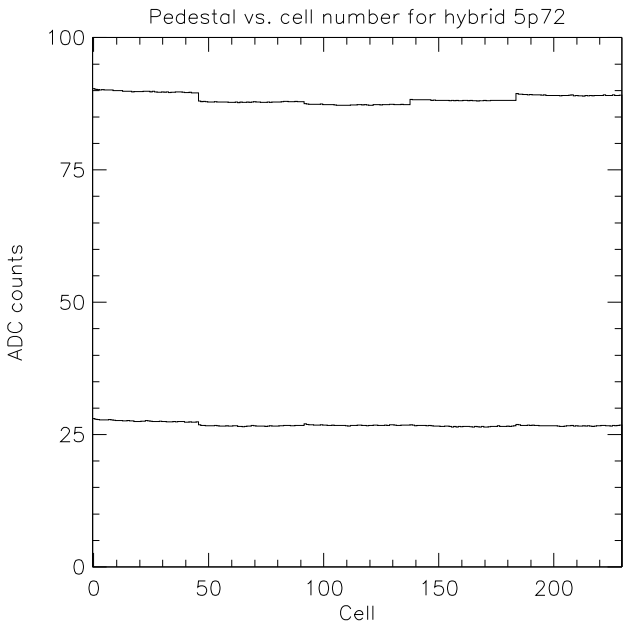
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

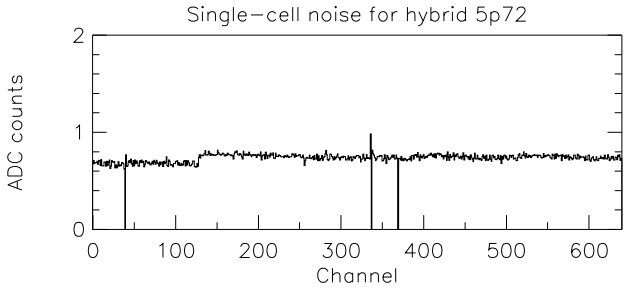
Pedestal vs. Pipeline Cell ID

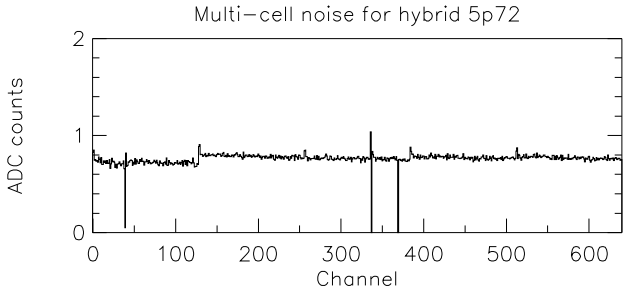


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

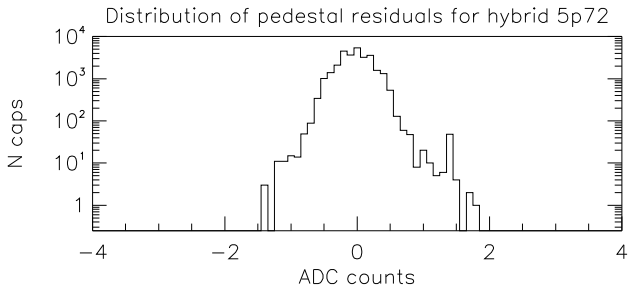
RMS Noise

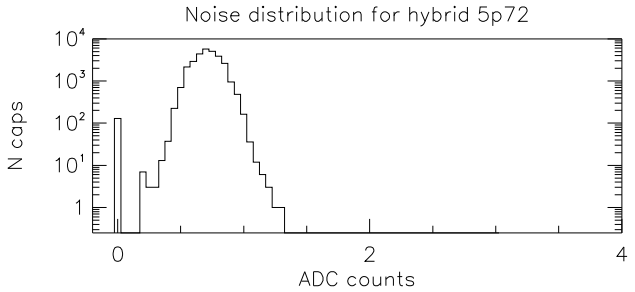




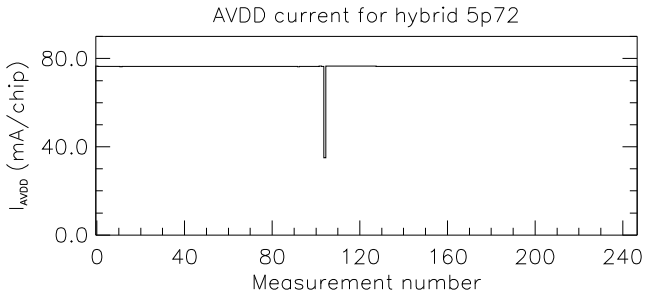
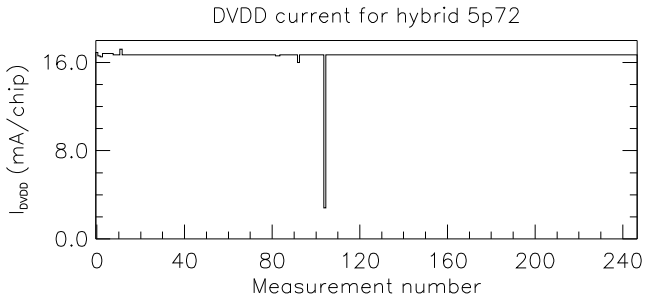
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in