Hybrid 5z145 Traveler

February 8, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: Bus1B open on chip 3, fixed with w/b to chip 2. FECLK open on chip 4, fixed with w/b to chip 5. AVDD open to finger 1 fixed with solder wire. Bus 0B open to chip 4 and 5; fixed with added wire between solder fields.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z145 has die: 100-006 100-007 100-008 100-009 100-010

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z145 classification info. Created 11:41:49 02/07/00

Hybrid 5z145 quality: fair
Chip classification: good good good good fair
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 4-22-15
Channels at pedestal needed for DCMS: 36.7 36.6 36.7 37.7 35.7
```

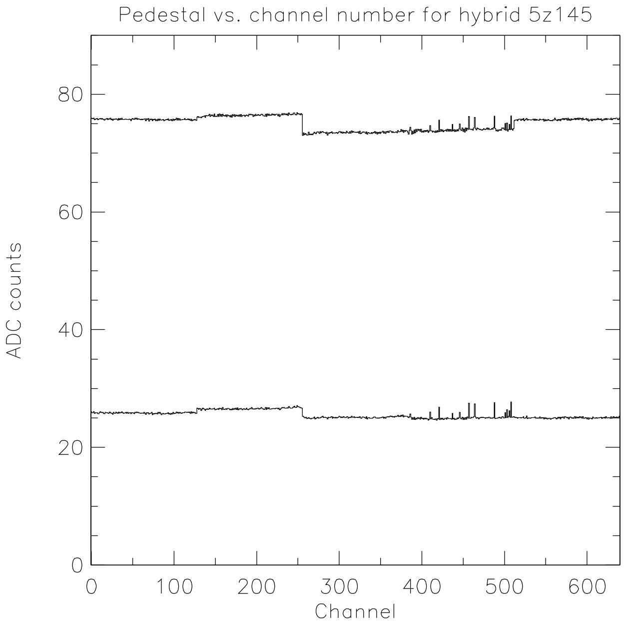
4 Comments

Encapsulated. HV tested. FE Au DVDD and DGND wirebond.

5 Pedestal

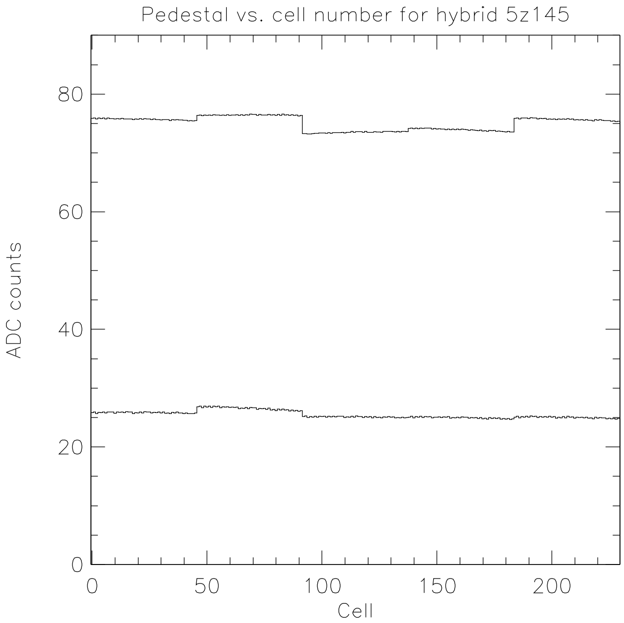
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

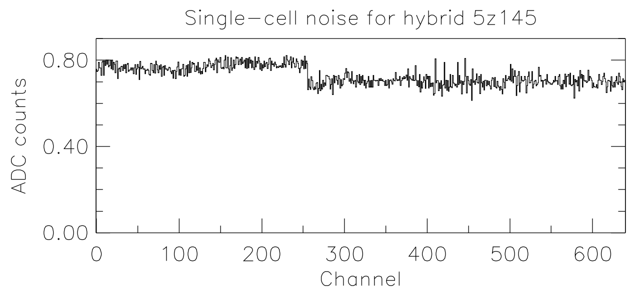
Pedestal vs. Pipeline Cell ID

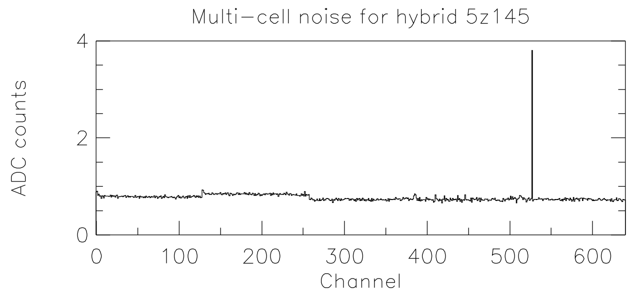


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

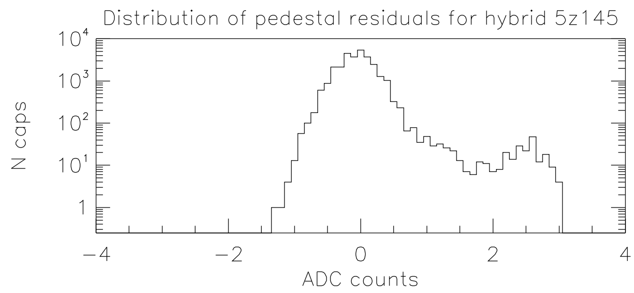
RMS Noise

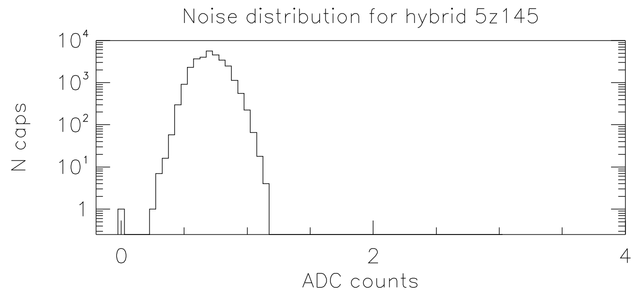




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in