Hybrid 5z153 Traveler

May 3, 2000

1 Connectivity

Repairs on shorts: Bus 7B shorted to GND; fixed by cutting 7B trace to chip 5. Bus 7B jumped from chip 4 to 5.

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z153 has die: 217-012 217-014 217-020 217-021 217-026

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z153 classification info. Created 12:22:03 02/09/00

Hybrid 5z153 quality: fair*
Chip classification: fair fair* fair fair fair
Bad channels (chip-channel): 0-53 1-74 1-104 1-121 2-14 3-13 3-86 4-28
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-1-88 0-1-89 0-14-87
   0-14-88 0-14-89 0-15-88 0-3-88 0-3-89 0-41-88 0-44-88 0-45-88
   0-5-88 2-44-23 3-11-67 3-3-33 3-3-64 3-3-65 3-34-49 4-12-48
Channels at pedestal needed for DCMS: 34.2 33.8 34.6 31.8 33.7
```

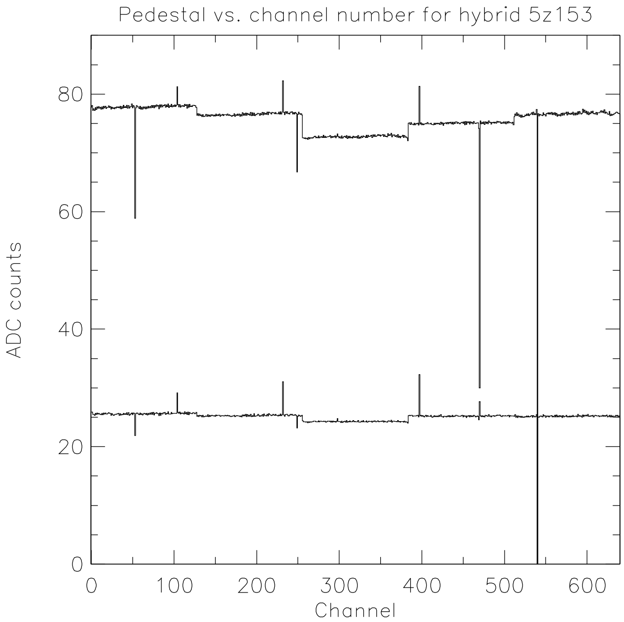
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

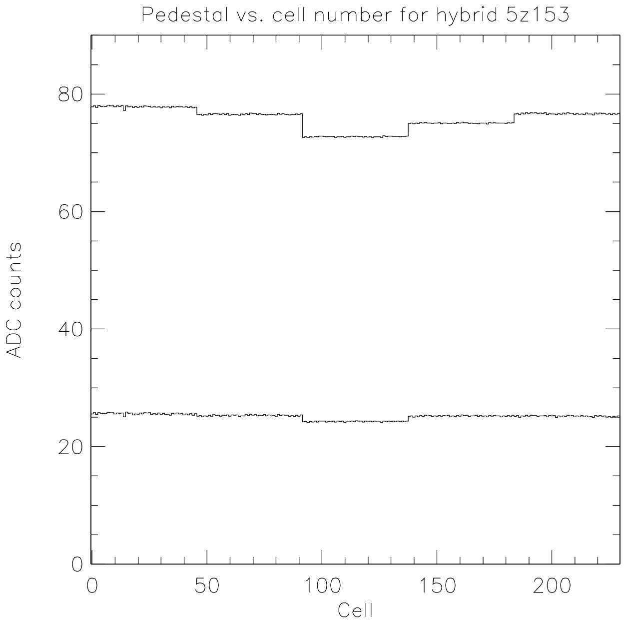
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

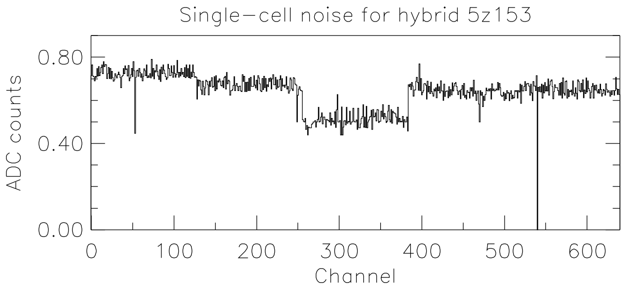
Pedestal vs. Pipeline Cell ID

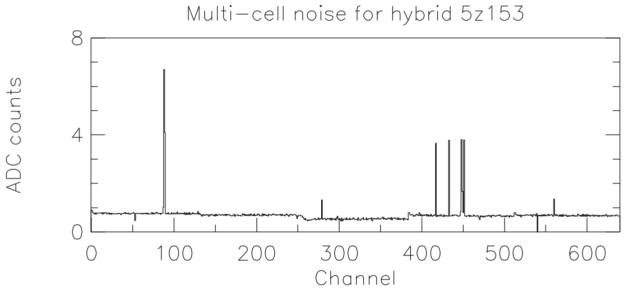


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

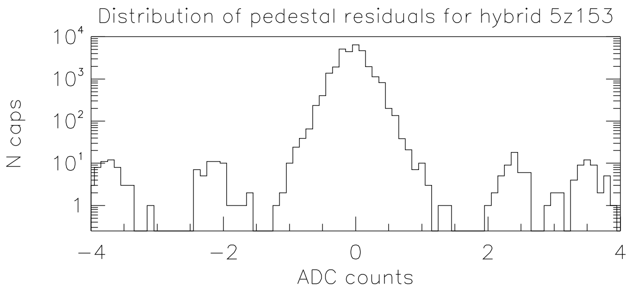
RMS Noise

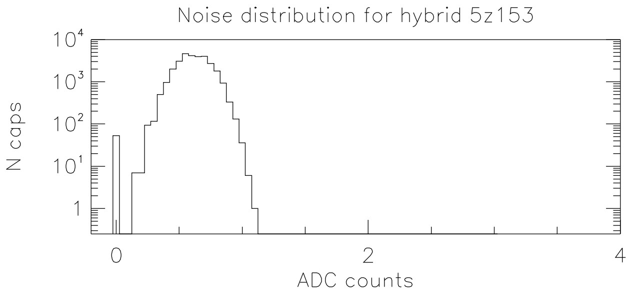




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in