Hybrid 5z18 Traveler

June 19, 2000

1 Connectivity

Repairs on shorts: HV bypassed with soldered wires.

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z18 has die: 181-112 181-113 181-118 181-119 181-120

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z18 classification info. Created 16:18:23 04/30/00

Hybrid 5z18 quality: fair*
Chip classification: fair fair good fair* good
Bad channels (chip-channel): 0-48 3-45 3-46 3-47 3-48
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-19-124 0-19-125 0-20-124
   0-23-124 0-23-125 0-24-124 0-26-124 0-26-125 0-28-124 0-28-125 0-30-124
   0-30-125 0-39-124 0-39-125 0-40-124 0-6-124 1-11-112 1-16-49 1-36-80
Channels at pedestal needed for DCMS: 33.5 32.6 30.7 31.3 33.7
```

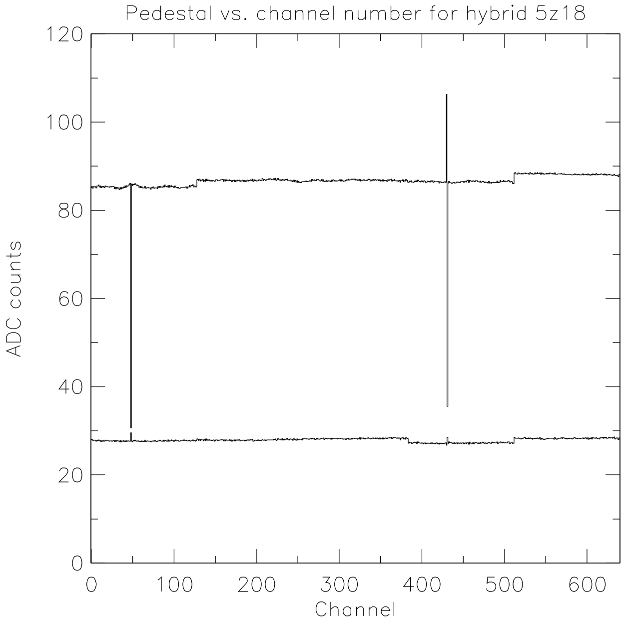
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

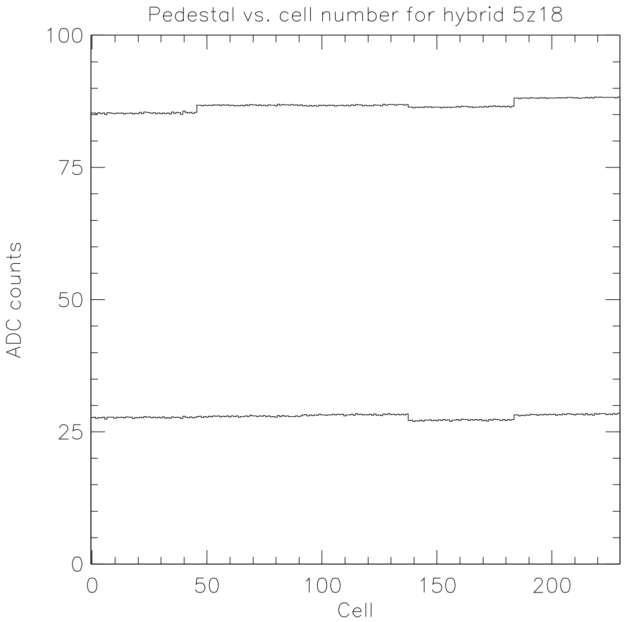
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

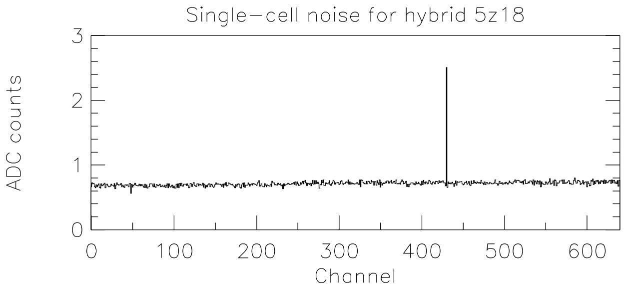
Pedestal vs. Pipeline Cell ID

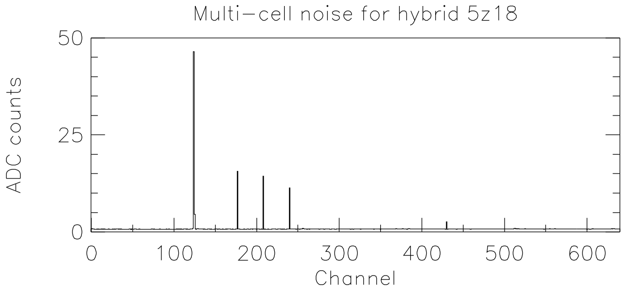


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

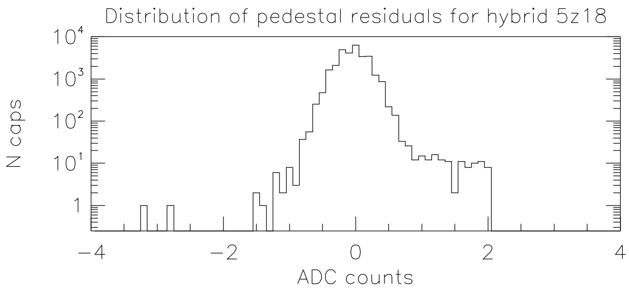
RMS Noise

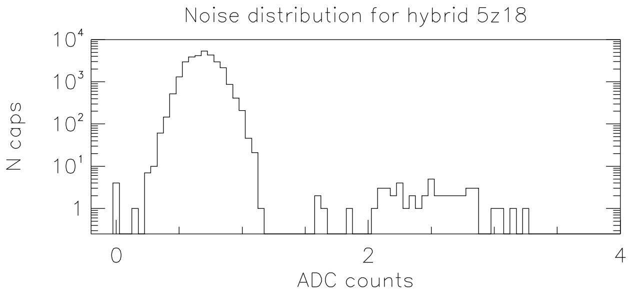




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in