Hybrid 5z192 Traveler

April 19, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z192 has die: 142-049 142-050 142-051 142-053 142-056

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z192 classification info. Created 14:46:03 03/03/00

Hybrid 5z192 quality: fair
Chip classification: good good fair good fair
Bad channels (chip-channel): 2-39 4-57
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-15-41 2-2-40 2-2-41
   2-28-40 2-28-41 2-29-41 2-3-41 2-32-40 2-32-41 2-33-41 2-35-40
   2-35-41 2-37-40 2-37-41 2-39-40 2-39-41 4-20-56 4-20-57 4-21-57
   4-24-56 4-24-57 4-25-57 4-27-56 4-27-57 4-29-56 4-29-57 4-31-56
   4-31-57 4-40-56 4-40-57 4-41-57 4-7-57
Channels at pedestal needed for DCMS: 31.7 31.7 31.7 33.7 34.4
```

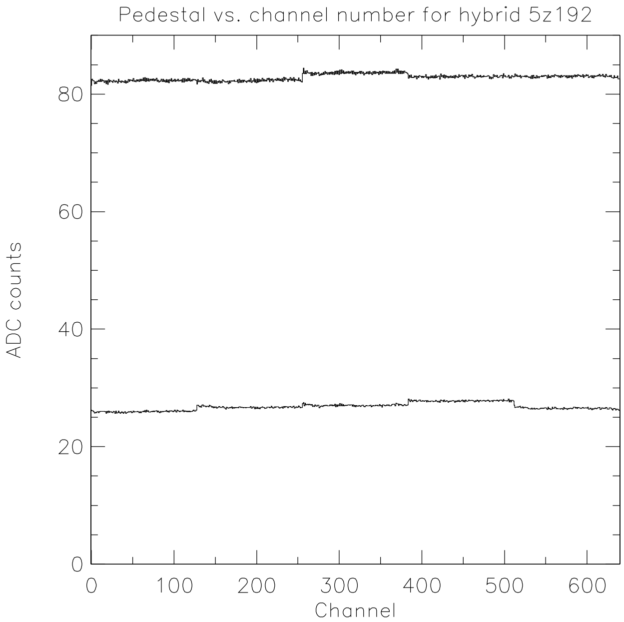
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

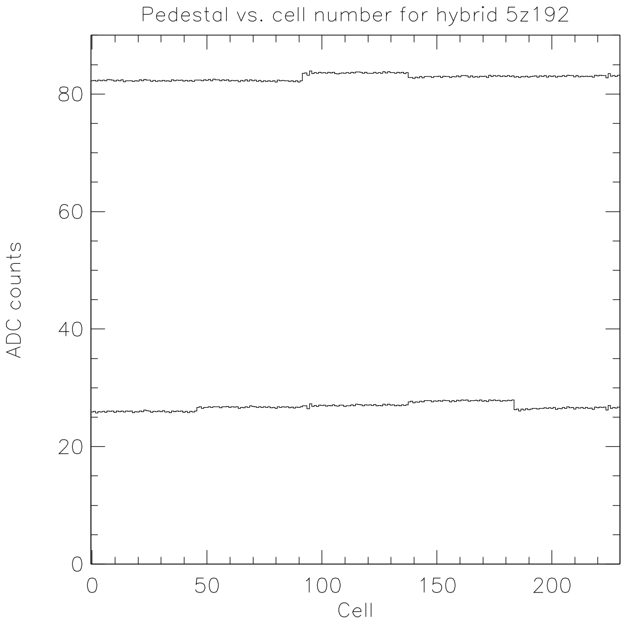
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

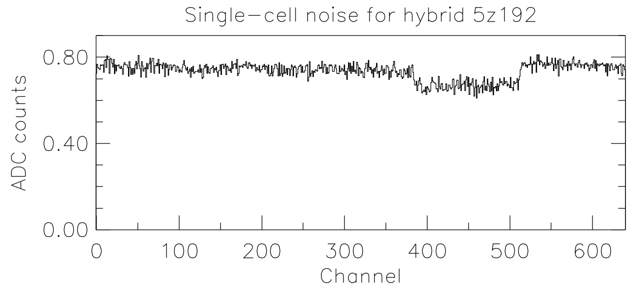
Pedestal vs. Pipeline Cell ID

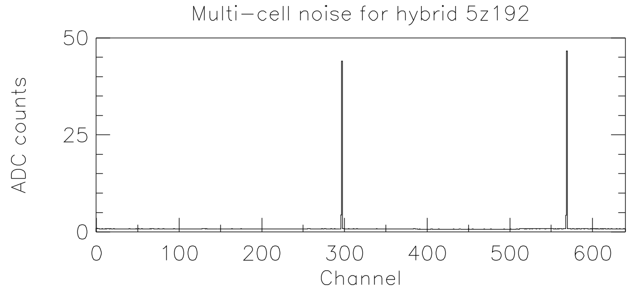


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

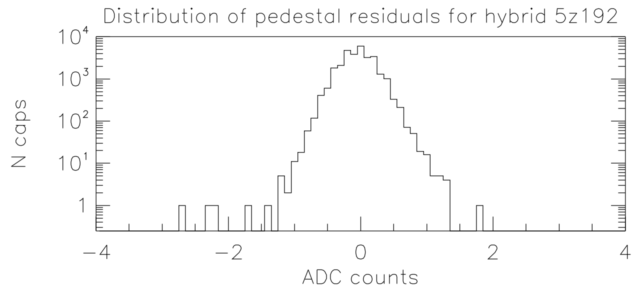
RMS Noise

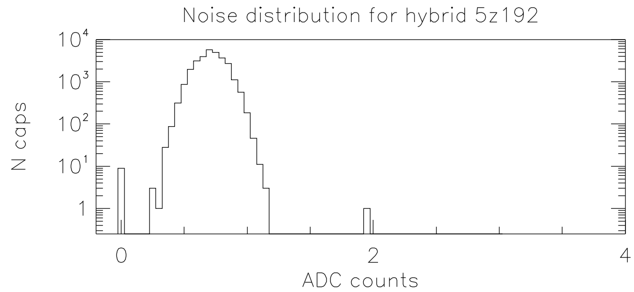




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in