Hybrid 5z50 Traveler

December 14, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z50 has die: 118-003 109-001 108-025 001-015 110-038

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z50 classification info. Created 20:18:39 10/25/99

Hybrid 5z50 quality: fair
Chip classification: good fair good good good
Bad channels (chip-channel): 1-109
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-36-110
Channels at pedestal needed for DCMS: 41.4 37.7 36.7 36.6 35.6
```

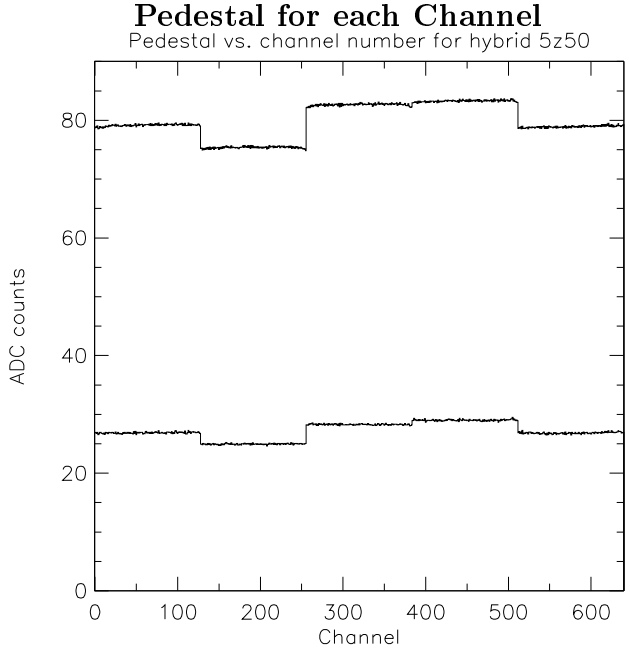
4 Comments

Chip 1 replaced with 118-3.
Has encapsulation.
Has redundant FE DVDD and DGND wirebonds.
HV Test.

5 Pedestal

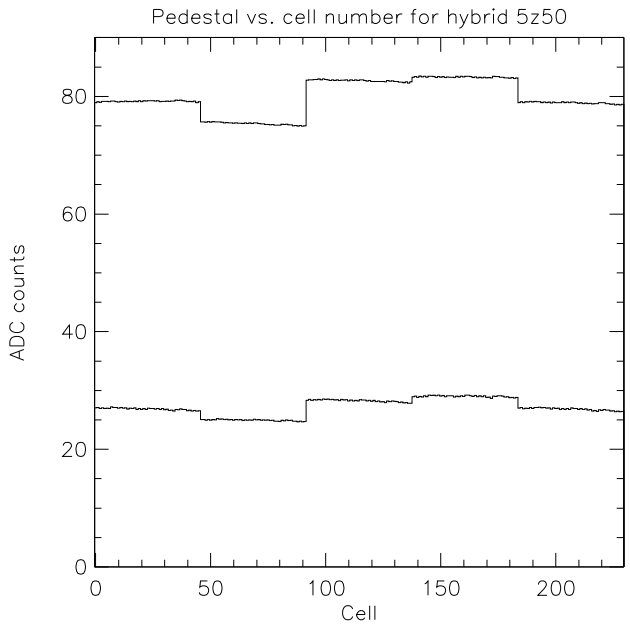
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

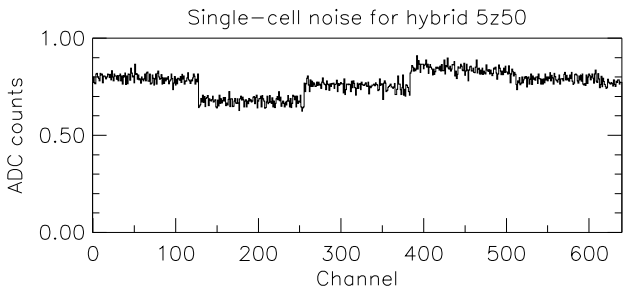
Pedestal vs. Pipeline Cell ID

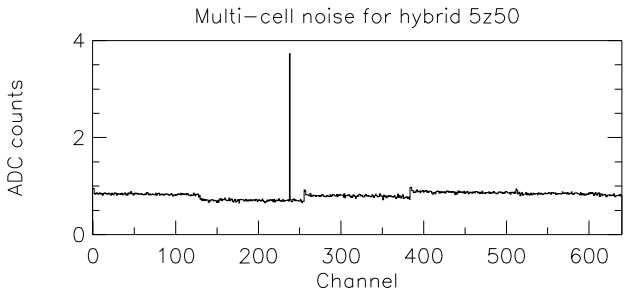


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

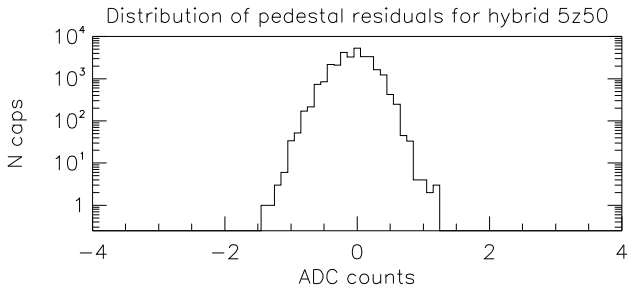
RMS Noise

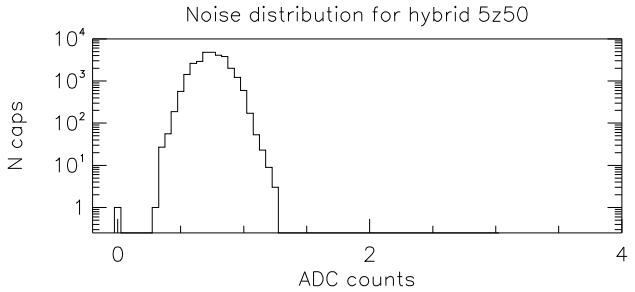




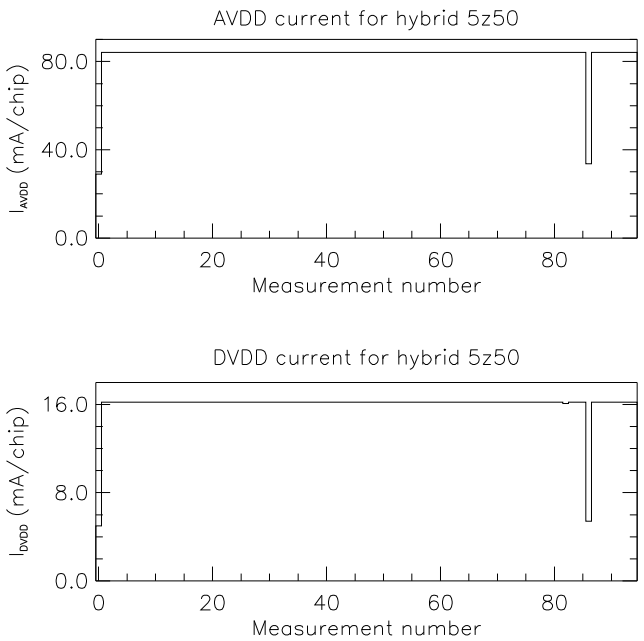
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in