Hybrid 5z56 Traveler

June 13, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z56 has die: 180-026 180-027 180-029 180-030 180-031

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z56 classification info. Created 10:54:51 06/12/00

Hybrid 5z56 quality: fair
Chip classification: good good fair good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-10-38 2-10-39 2-11-39
   2-13-38 2-13-39 2-15-38 2-15-39 2-17-38 2-17-39 2-26-38 2-26-39
   2-27-39 2-39-39 2-7-39
Channels at pedestal needed for DCMS: 32.6 31.6 30.7 33.3 31.6
```

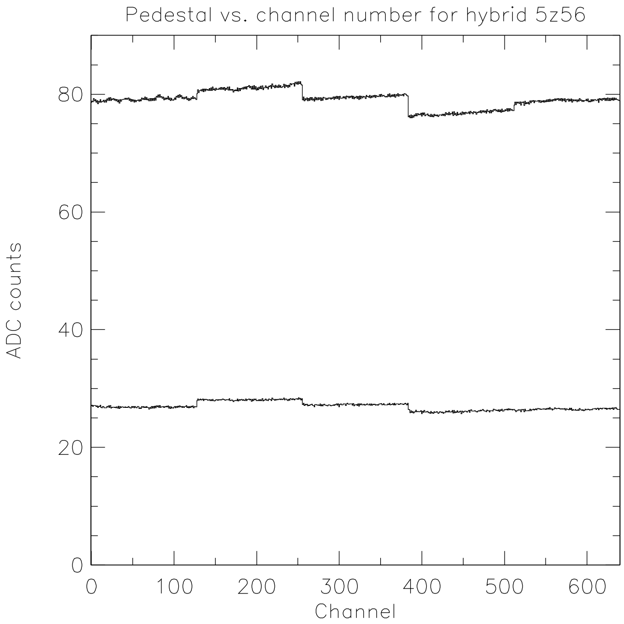
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

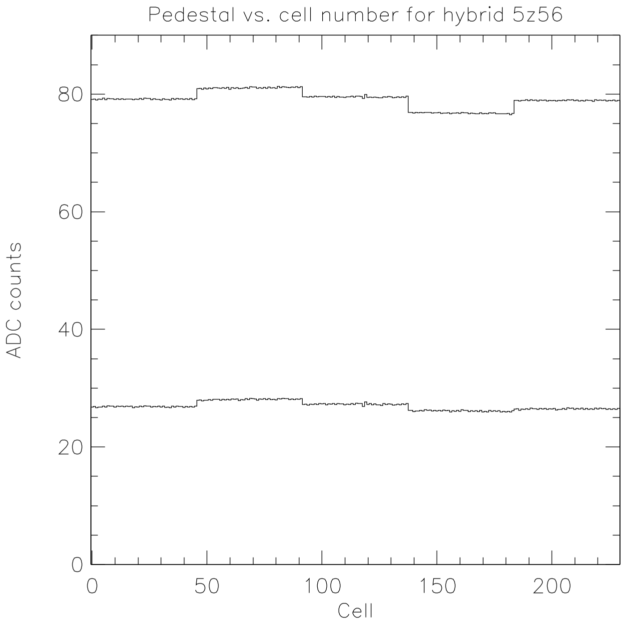
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

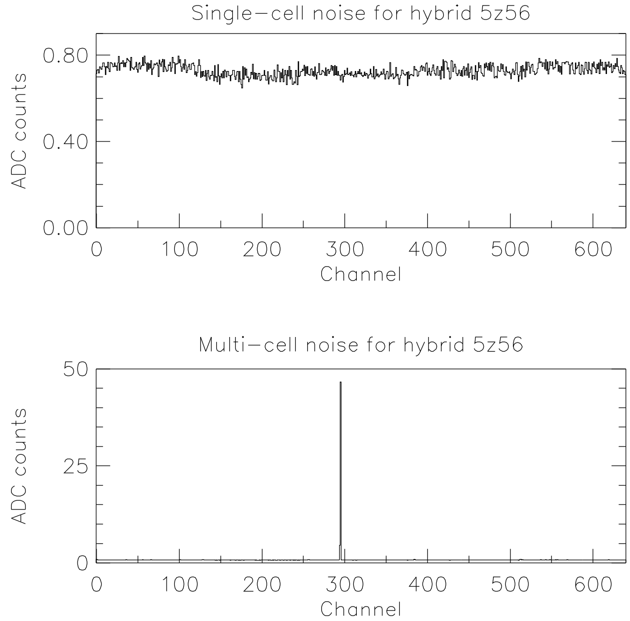
Pedestal vs. Pipeline Cell ID



6 Noise

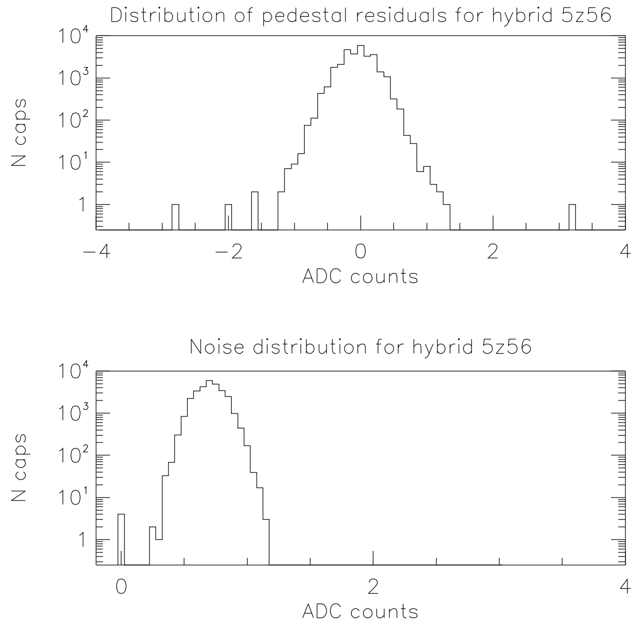
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in