Hybrid 5z96 Traveler

December 8, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z96 has die: 096-012 096-013 096-016 096-017 096-018

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z96 classification info. Created 14:04:19 11/27/99

Hybrid 5z96 quality: fair
Chip classification: good good good fair good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-1-118 3-1-119 3-10-117
   3-10-118 3-10-119 3-11-119 3-2-119 3-23-119 3-37-119 3-40-118 3-40-119
   3-41-119 3-43-118 3-43-119 3-45-118 3-45-119
Channels at pedestal needed for DCMS: 37.6 36.7 35.6 36.6 34.6
```

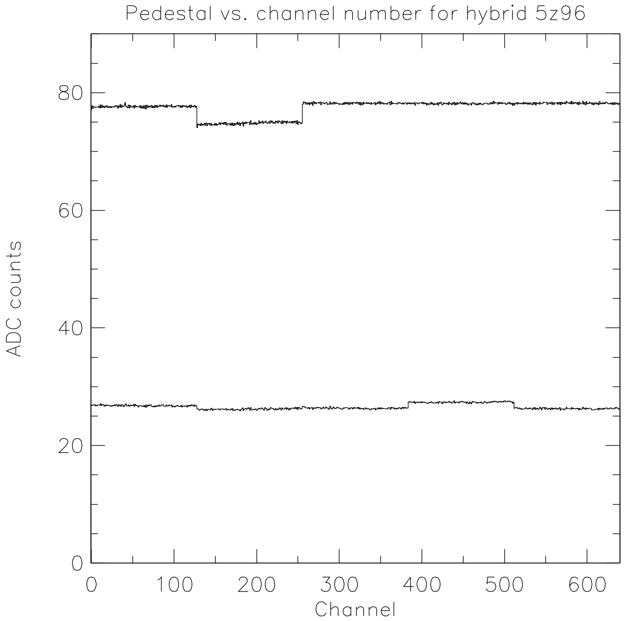
4 Comments

Has redundant FE DVDD and DGND wirebonds.

5 Pedestal

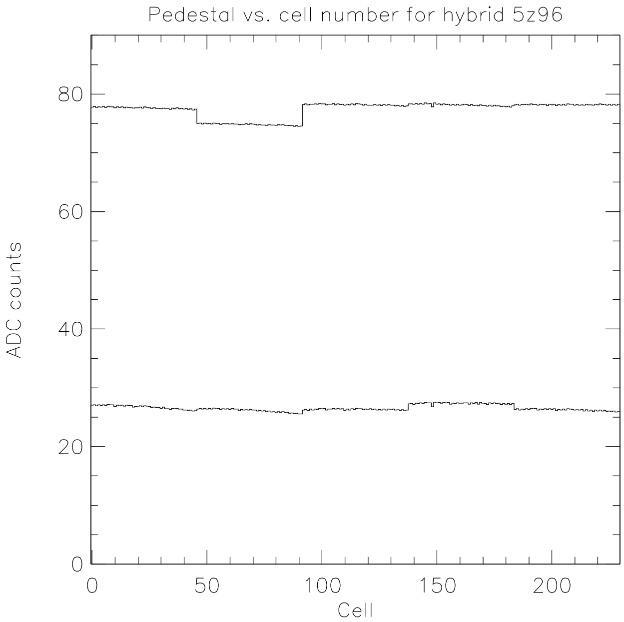
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

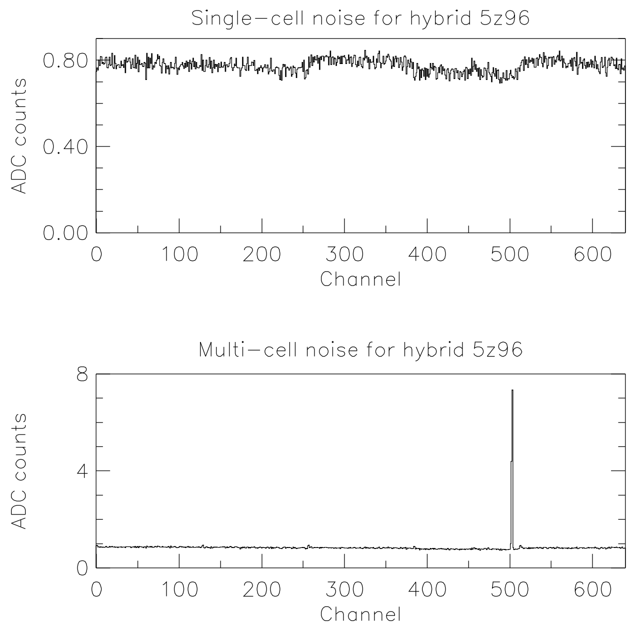
Pedestal vs. Pipeline Cell ID



6 Noise

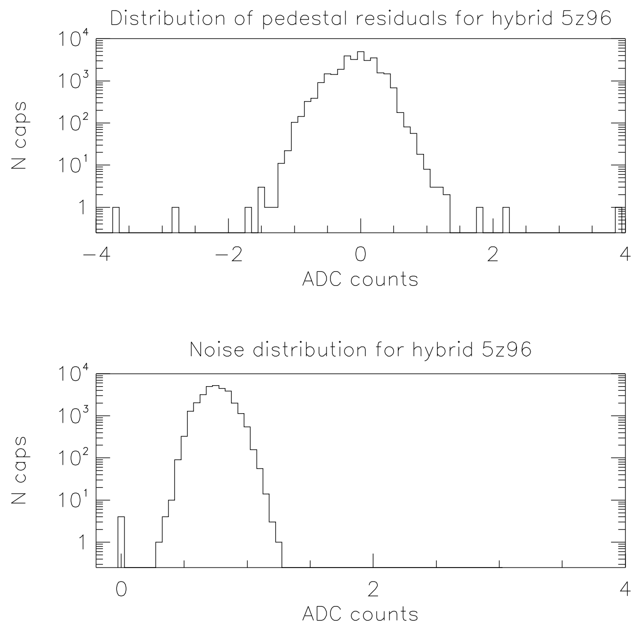
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in