Hybrid 6p102 Traveler

January 25, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: Bus 3B open on chips 5 and 6. Fixed with wirebonds.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P102 has die: 215-108 215-110 215-111 215-113 215-114 215-115

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p102 classification info. Created 12:52:58 01/24/00

Hybrid 6p102 quality: fair
Chip classification: fair fair good good good fair
Bad channels (chip-channel): 1-60 5-37
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-14-106
Channels at pedestal needed for DCMS: 30.5 31.6 35.5 35.7 33.7 34.2
```

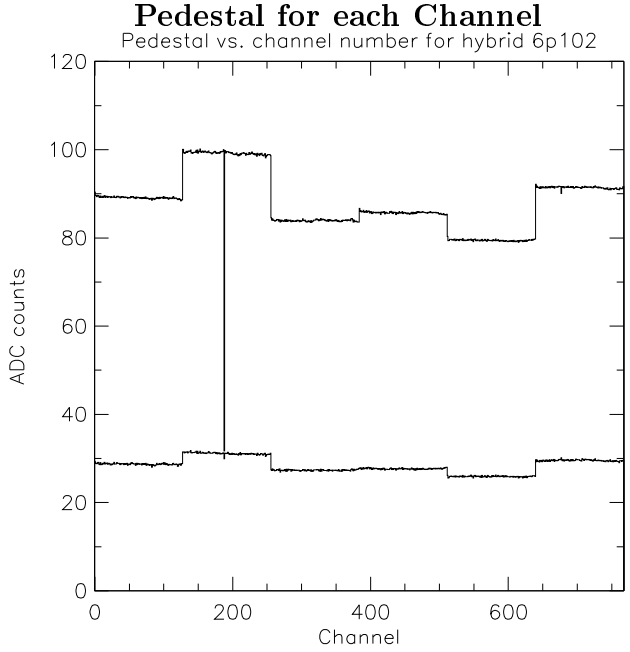
4 Comments

Encapsulated.
FE DV finger gold bonds.
HV tested.

5 Pedestal

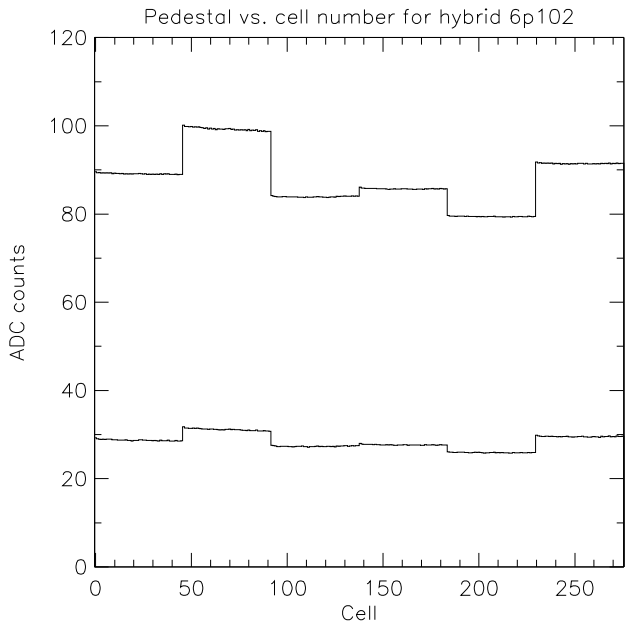
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

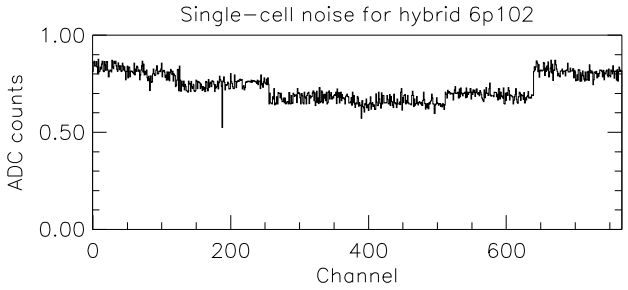
Pedestal vs. Pipeline Cell ID

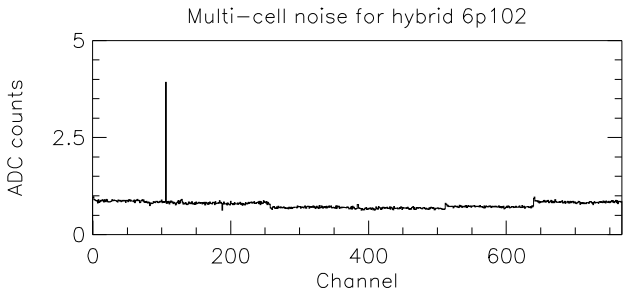


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

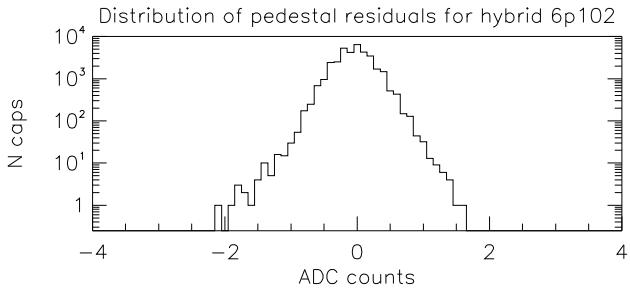
RMS Noise

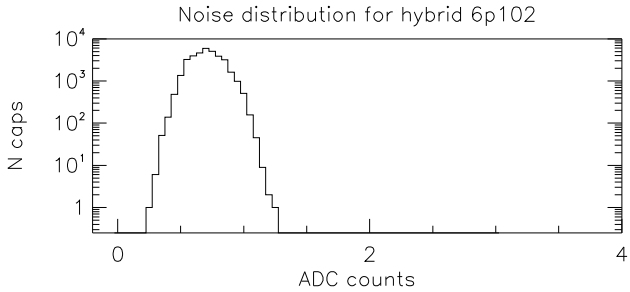




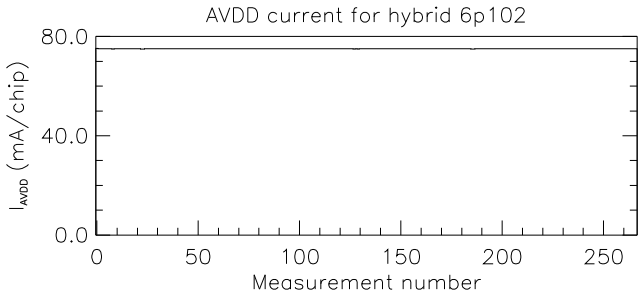
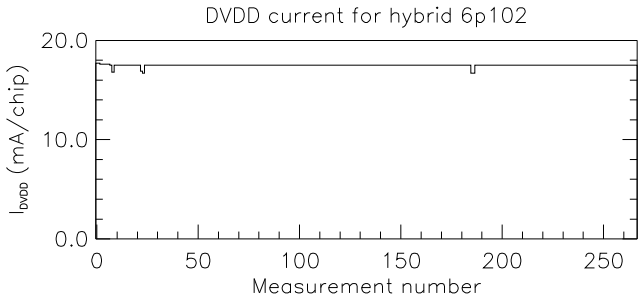
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in