Hybrid 6p110 Traveler

January 11, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P110 has die: 195-087 195-088 195-089 195-090 195-092 195-094

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p110 classification info. Created 14:06:43 01/10/00

Hybrid 6p110 quality: fair
Chip classification: good fair good good fair good
Bad channels (chip-channel): 4-25
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-24-49 1-34-67
Channels at pedestal needed for DCMS: 37.6 32.9 33.7 34.6 33.6 36.5
```

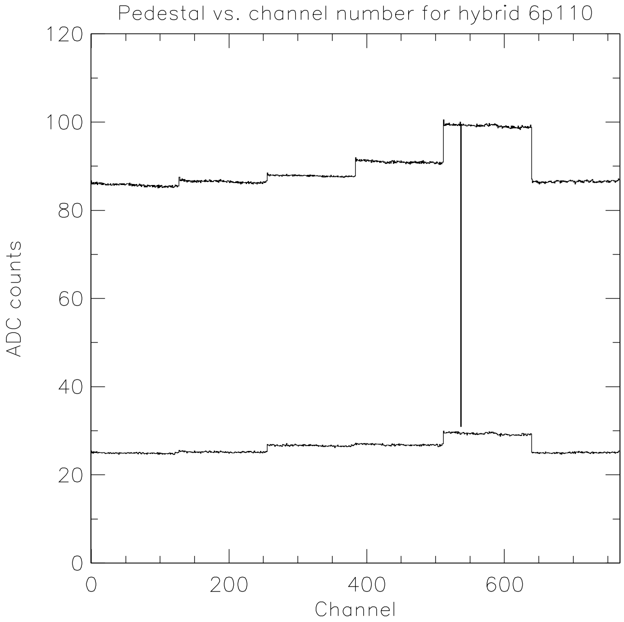
4 Comments

Has Au FE DVDD, DGND bonds.
HV test.

5 Pedestal

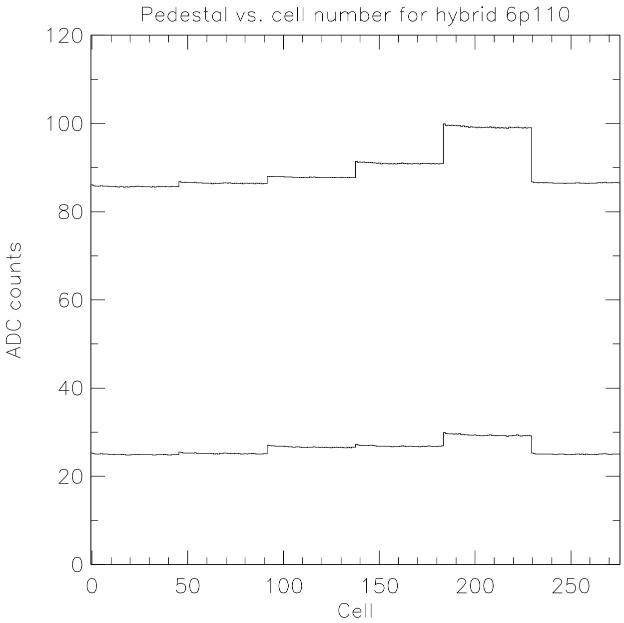
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

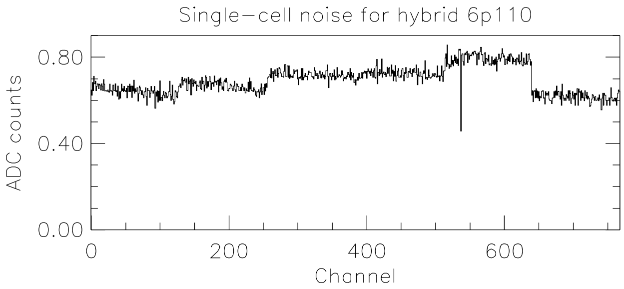
Pedestal vs. Pipeline Cell ID

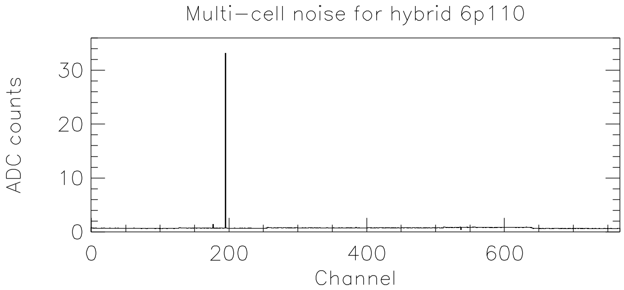


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

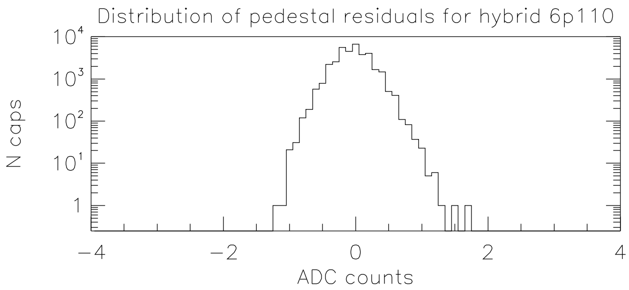
RMS Noise

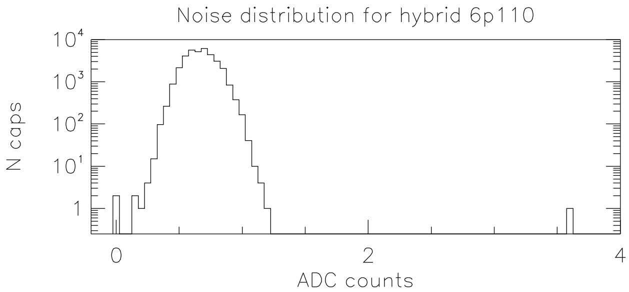




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in