Hybrid 6p123 Traveler

January 7, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: Wirebond from P0 to gold trace below, then wire added between that and BN in the solder field.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P123 has die: 194-048 194-052 194-053 194-054 194-055 194-056

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p123 classification info. Created 14:04:25 01/07/00

Hybrid 6p123 quality: fair
Chip classification: good fair good good fair fair
Bad channels (chip-channel): 1-67 4-2 5-53
Bad cells: none
Random bad capacitors (chip-cell-channel): 5-10-56 5-26-56 5-26-57
   5-27-56 5-39-56
Channels at pedestal needed for DCMS: 32.6 32.4 34.6 34.6 34.3 31.4
```

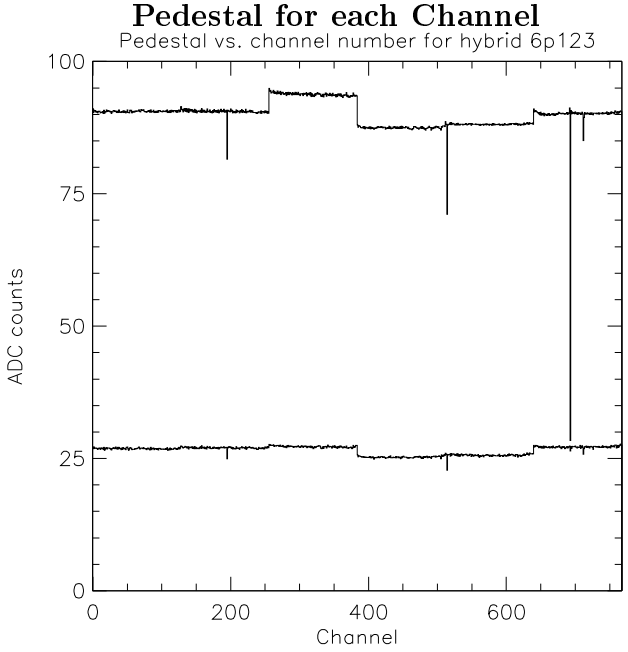
4 Comments

Has Au FE DVDD, DGND bonds.
HV test.

5 Pedestal

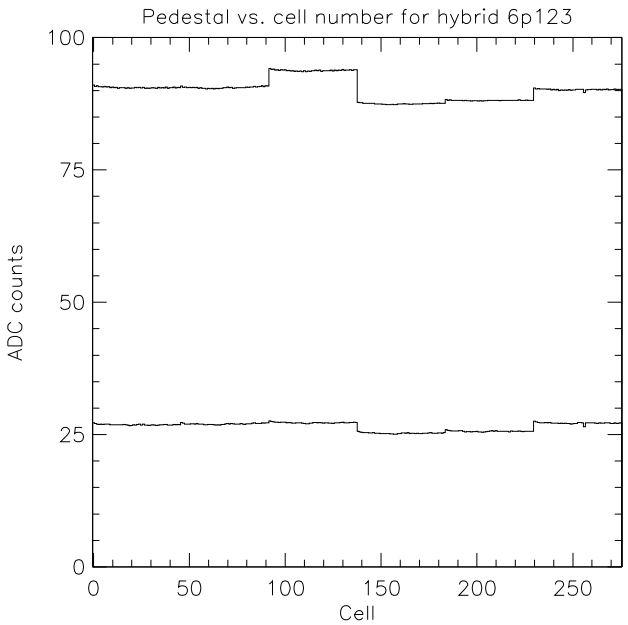
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

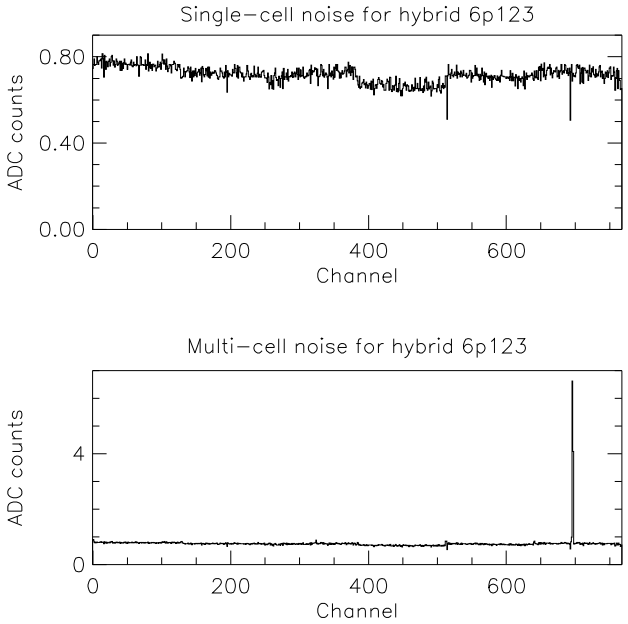
Pedestal vs. Pipeline Cell ID



6 Noise

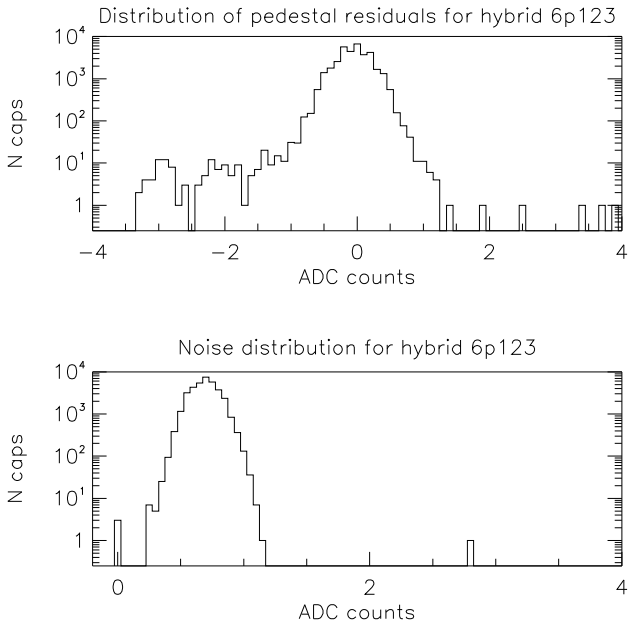
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise

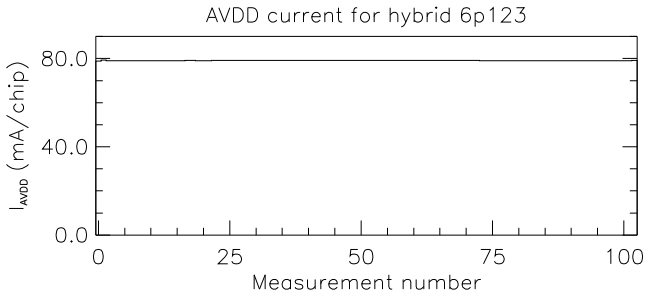
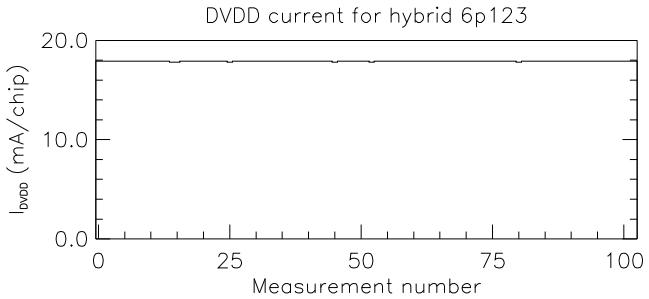


The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in