Hybrid 6p206 Traveler

June 6, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens: AVDD chip 3, HV- with soldered wires.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P206 has die: 152-054 152-055 152-056 152-057 152-061 152-062

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p206 classification info. Created 10:28:47 05/31/00

Hybrid 6p206 quality: fair
Chip classification: good fair good good good fair
Bad channels (chip-channel): 5-42 5-43
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-31-101 1-31-102 1-31-103
   1-32-102 5-16-2 5-27-18 5-27-69 5-37-7 5-39-53 5-39-93
Channels at pedestal needed for DCMS: 29.7 30.6 29.7 29.9 28.8 31.6
```

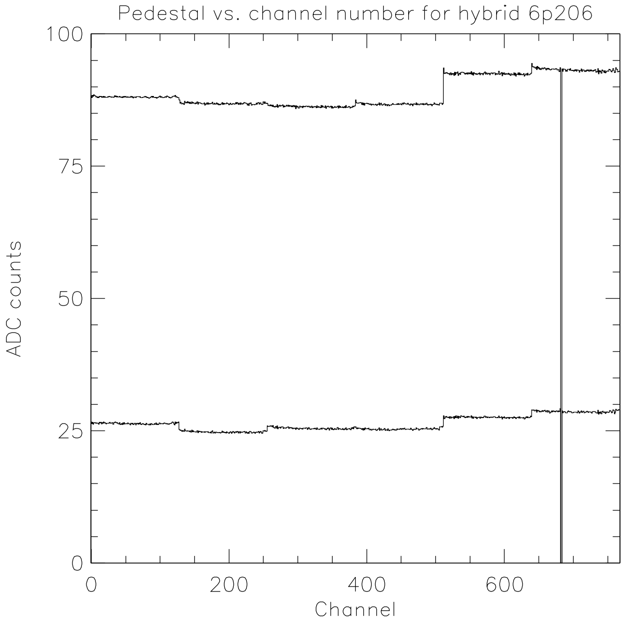
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

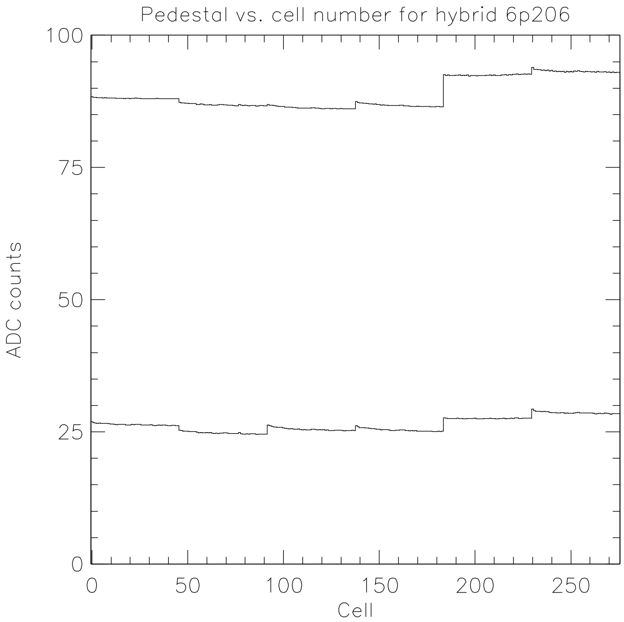
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

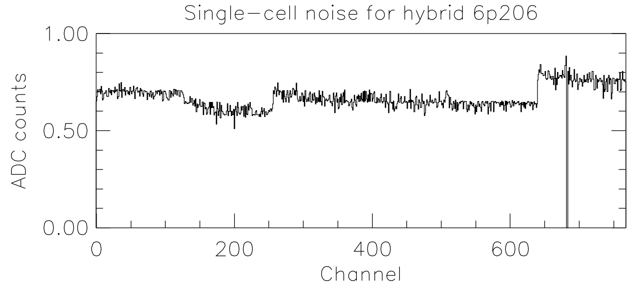
Pedestal vs. Pipeline Cell ID

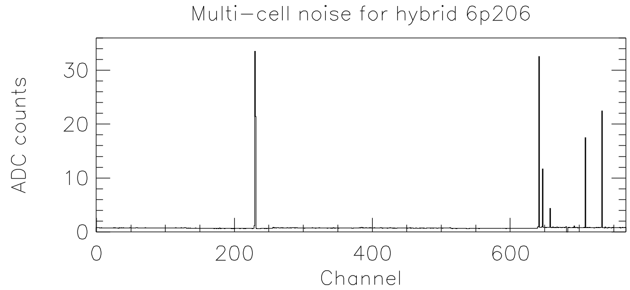


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

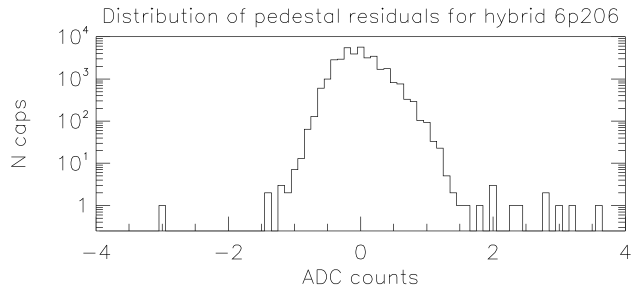
RMS Noise

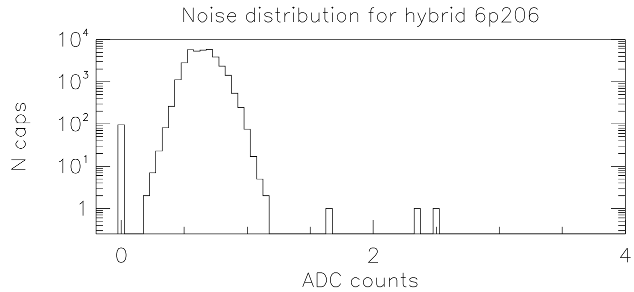




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in