# Hybrid 6p47 Traveler

March 21, 2000

## 1 Connectivity

Repairs on shorts:
Fixes for opens:

- Bus0 and Bus4B opens on chip 5 fixed by jumping to chip 4.
- AVDD solder pad on capacitor at C6 missing. Fixed with wire to spare trace and w/b to 1st finger.
- HV- open to left 3-chip side. Fixed with wire from HV- solder pad at R11B to HV resistor on left at R11A.

## 2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P47 has die: 114-014 114-015 114-017 114-018 047-022 115-030

## 3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p47 classification info. Created 16:05:43 03/06/00

Hybrid 6p47 quality: good
Chip classification: good good good good good good
Bad channels: none
Bad cells: none
Random bad capacitors: none
Channels at pedestal needed for DCMS: 35.6 38.6 36.8 35.7 33.6 36.6
```

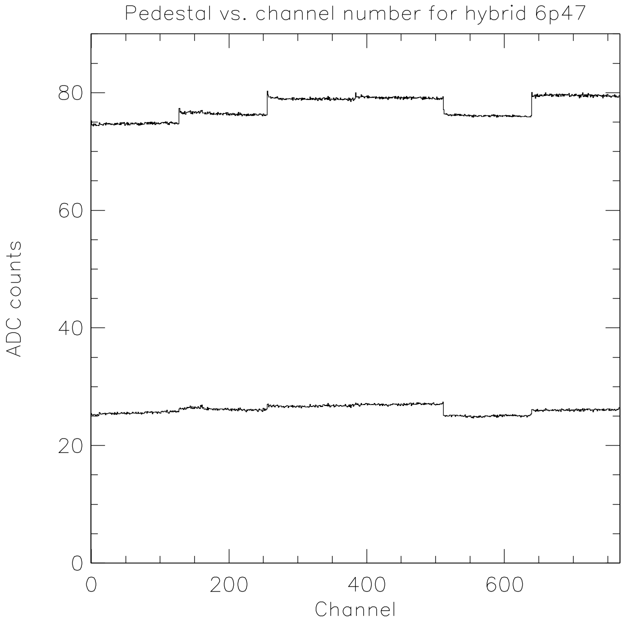
# 4 Comments

Encapsulated. HV tested. Has Au FE DVDD and DGND wirebonds.

# 5 Pedestal

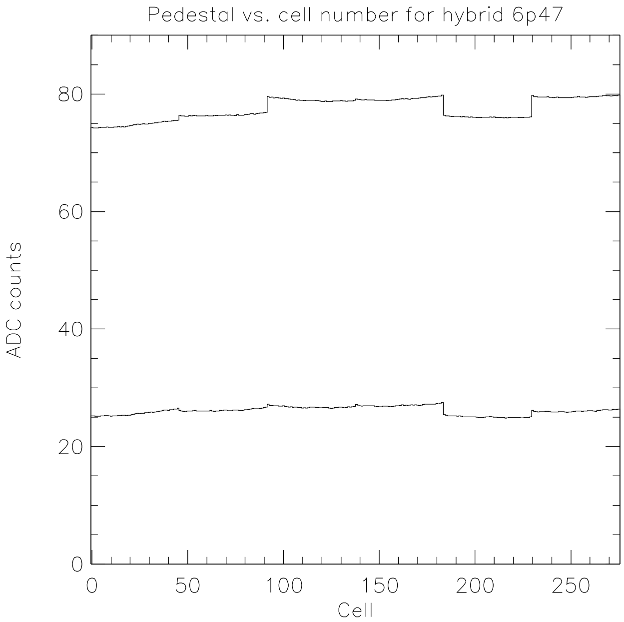
The following plot shows the pedestals vs. channel number with and without charge injection:

**Pedestal for each Channel**




The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

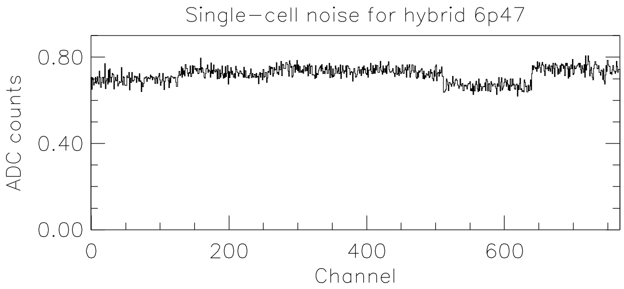
**Pedestal vs. Pipeline Cell ID**

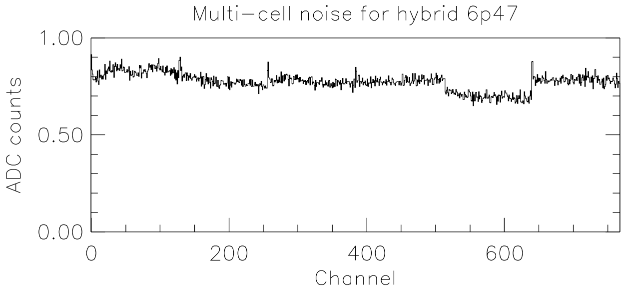


## 6 Noise

The following plots show the single-cell and multi-cell RMS noise:

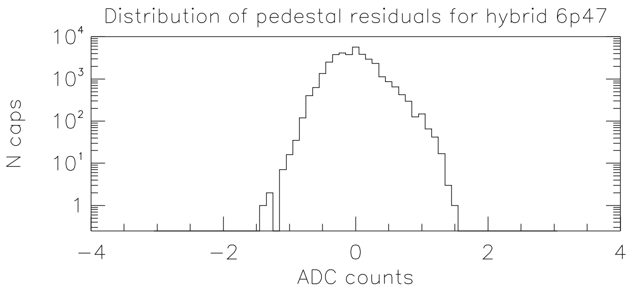
**RMS Noise**

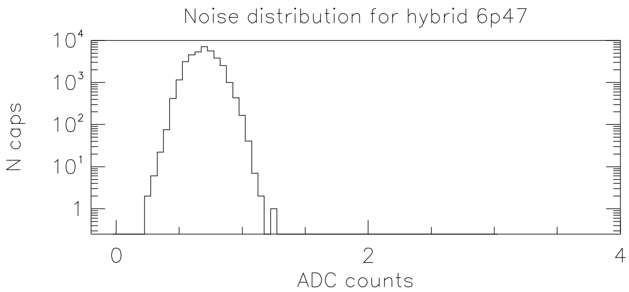



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

**Distribution of Pedestals and Noise**



# 7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

**Supply Currents During Burn-in**