Hybrid 6p60 Traveler

January 21, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: Bus1B, OBDV, L1A all open on chip 4, fixed with wire bonds. PRD1, PRD2 open to 2nd half of hybrid, fixed with wires.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P60 has die: 167-006 167-009 167-012 167-002 167-018 167-025

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p60 classification info. Created 16:58:17 01/17/00

Hybrid 6p60 quality: fair
Chip classification: fair fair fair fair good fair
Bad channels (chip-channel): 2-59
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-1-101 0-26-127 0-26-50
   0-3-127 1-28-83 1-9-84 2-40-31 3-26-127 5-7-126
Channels at pedestal needed for DCMS: 34.6 34.7 34.6 35.7 36.5 32.7
```

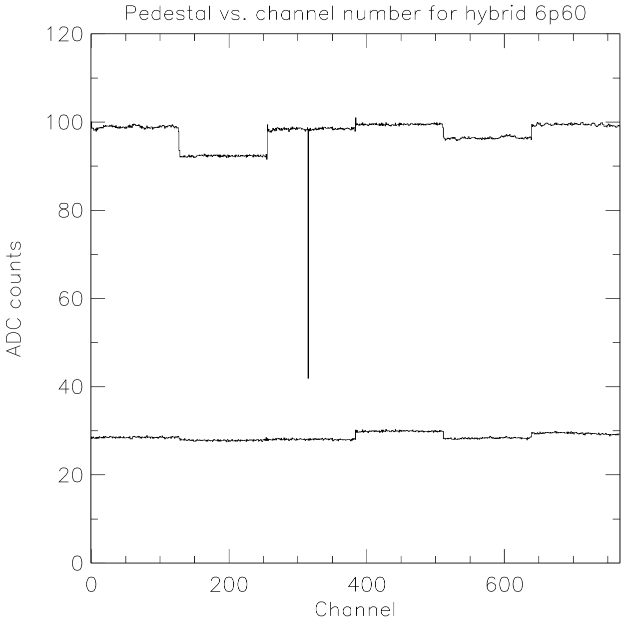
4 Comments

Hybrid operated through thermal-cycles for 1 month to test reliability of lot 9 and 12 die. Redundant FE DV bonds. Encapsulated.

5 Pedestal

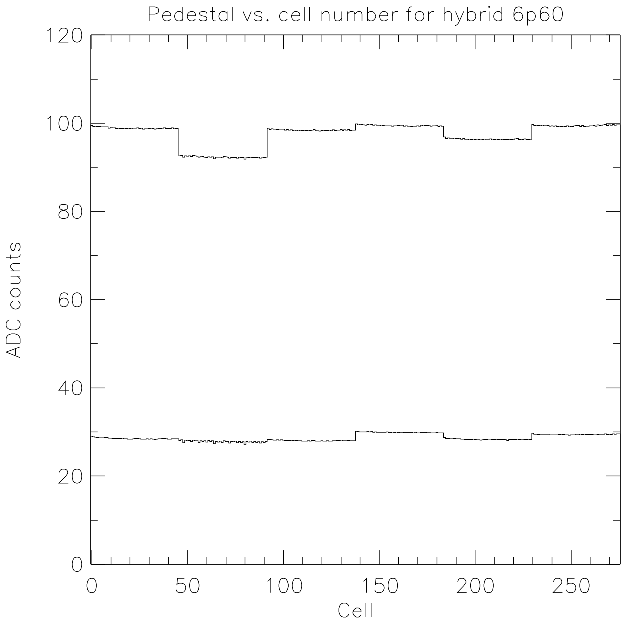
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

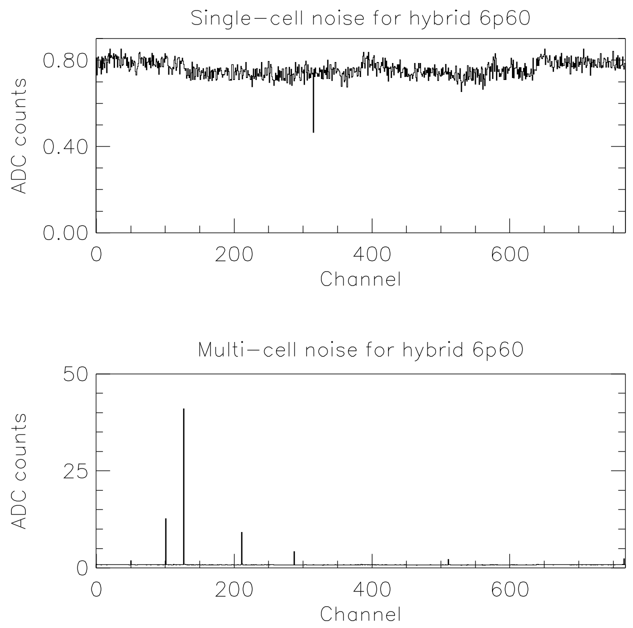
Pedestal vs. Pipeline Cell ID



6 Noise

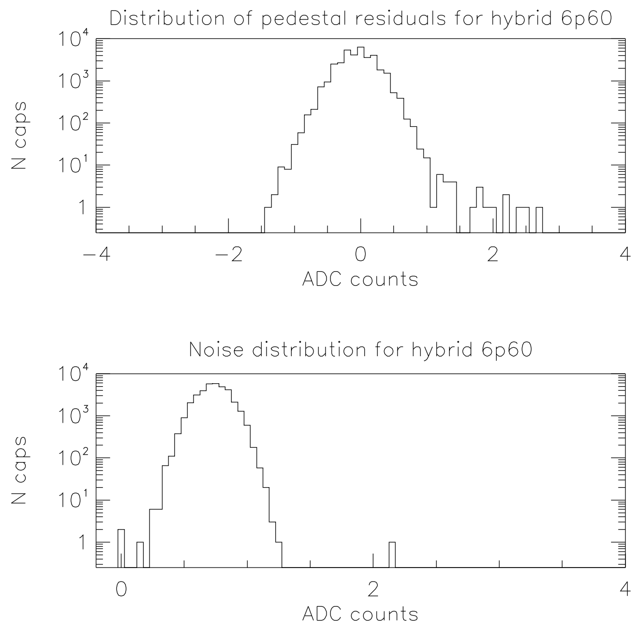
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in