Hybrid 6p99 Traveler

January 21, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: FE clk open fixed with soldered wire from cable to termination.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 6P99 has die: 184-001 184-004 184-002 184-013 184-003 184-020

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 6p99 classification info. Created 17:21:12 01/17/00

Hybrid 6p99 quality: fair
Chip classification: fair fair good fair good fair
Bad channels (chip-channel): 3-107
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-25-0 1-15-57 1-15-58
   3-29-25 5-27-20 5-45-25
Channels at pedestal needed for DCMS: 31.6 31.6 35.6 34.2 30.7 36.7
```

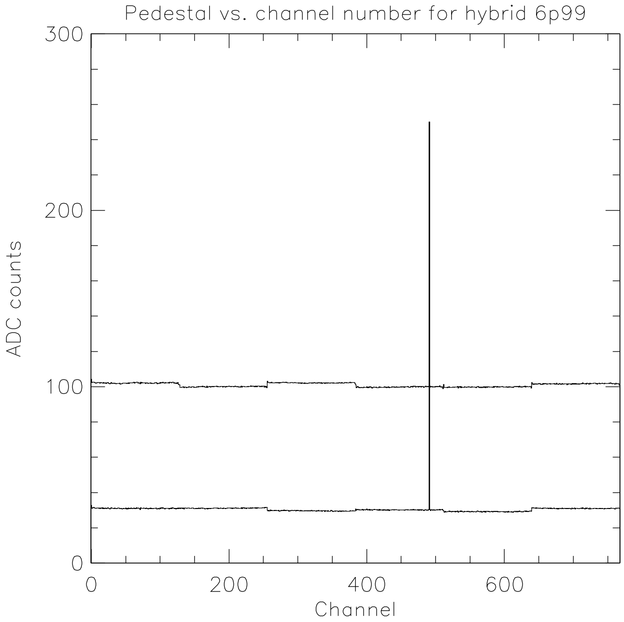
4 Comments

Hybrid operated through thermal-cycles for 1 month to test reliability of lot 9 and 12 die. Redundant FE DV bonds. Encapsulated.

5 Pedestal

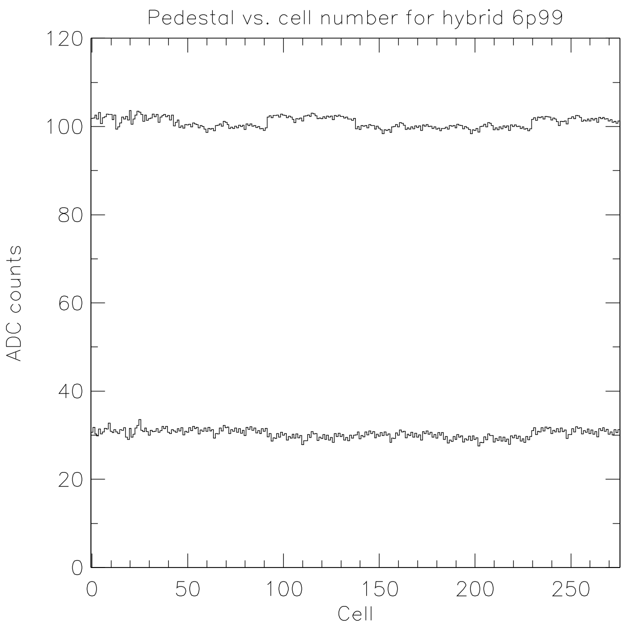
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

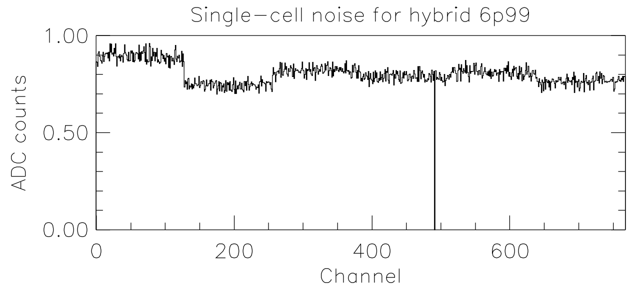
Pedestal vs. Pipeline Cell ID

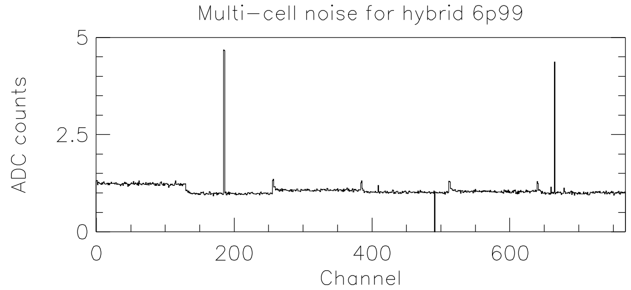


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

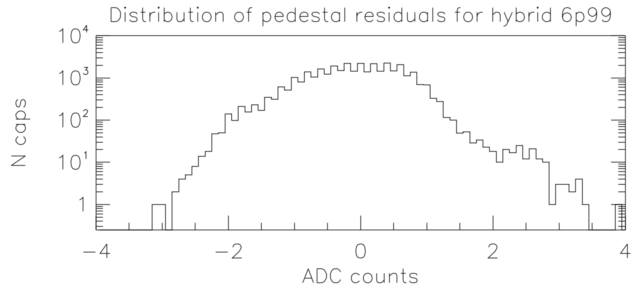
RMS Noise

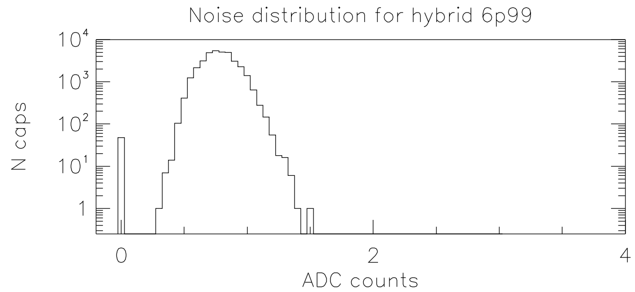




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in