Hybrid 7p140 Traveler

June 15, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens: Right 2 chip FE clock low with solder wire.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P140 has die: 157-066 157-068 224-036 157-072 157-073 157-075 157-076

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p140 classification info. Created 09:29:00 06/15/00

Hybrid 7p140 quality: fair
Chip classification: fair good fair good good good good
Bad channels (chip-channel): 0-39 0-59 2-39 2-99
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-34-102 0-34-111 0-34-116
   0-34-122 0-34-124 0-34-15 0-34-50 0-34-52 0-34-55 0-34-63 0-34-65
   0-34-66 0-34-72 0-34-76 0-34-83 0-34-87 0-42-71
Channels at pedestal needed for DCMS: 29.6 32.7 30.3 31.7 30.7 31.5 33.4
```

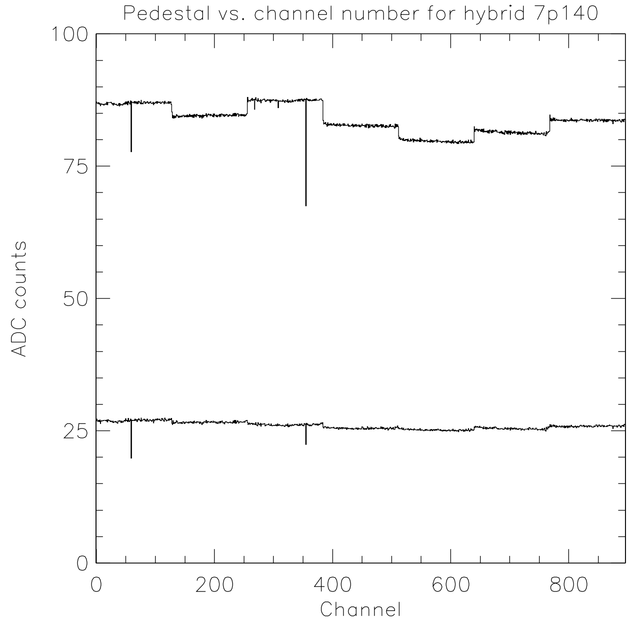
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

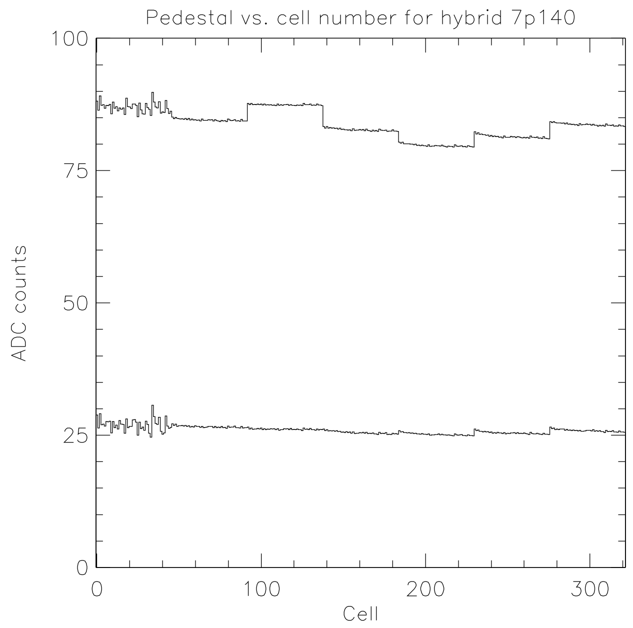
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

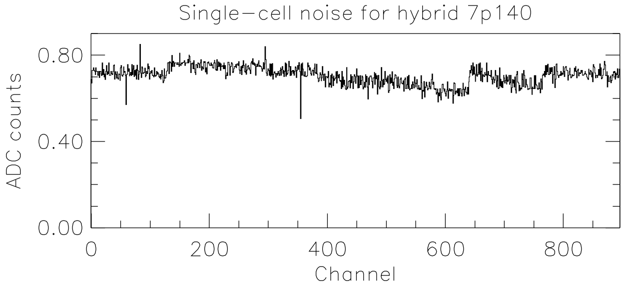
Pedestal vs. Pipeline Cell ID

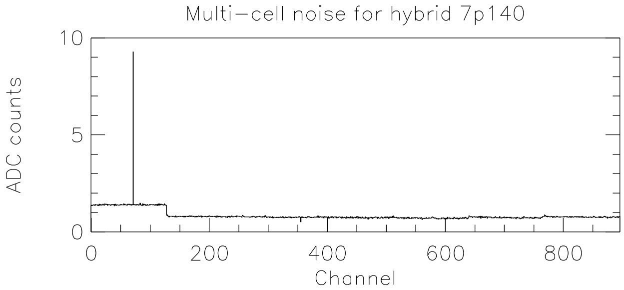


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

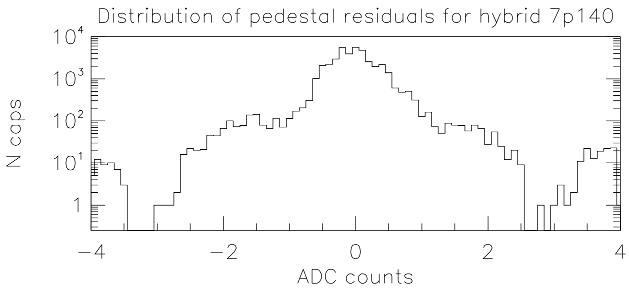
RMS Noise

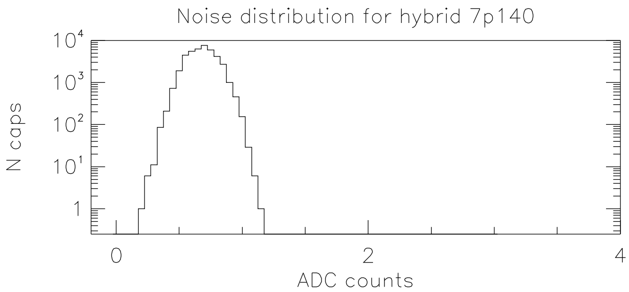




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in