Hybrid 7p170 Traveler

February 8, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:
HV+ open from R11A solder pad on the 3-chip sub-hybrid to the (0 Ohm) resistor on R5A on the neighboring 2-chip sub-hybrid. This was fixed with a wire.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P170 has die: 175-051 175-052 175-053 175-054 175-055 175-056 175-057

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p170 classification info. Created 09:07:27 02/07/00

Hybrid 7p170 quality: fair
Chip classification: fair good good fair good fair fair
Bad channels (chip-channel): 0-37 6-22
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-43-28 5-24-5 5-33-84
   6-42-21 6-44-49
Channels at pedestal needed for DCMS: 30.3 34.7 30.7 32.7 32.7 33.7 34.7
```

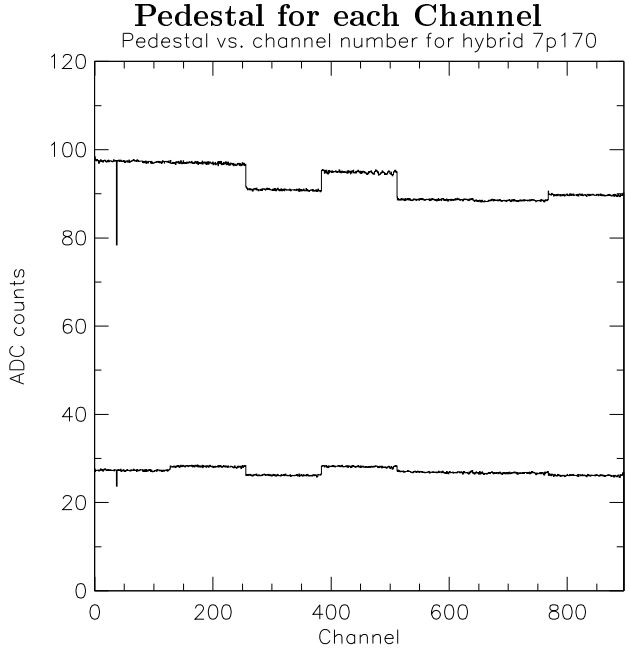
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

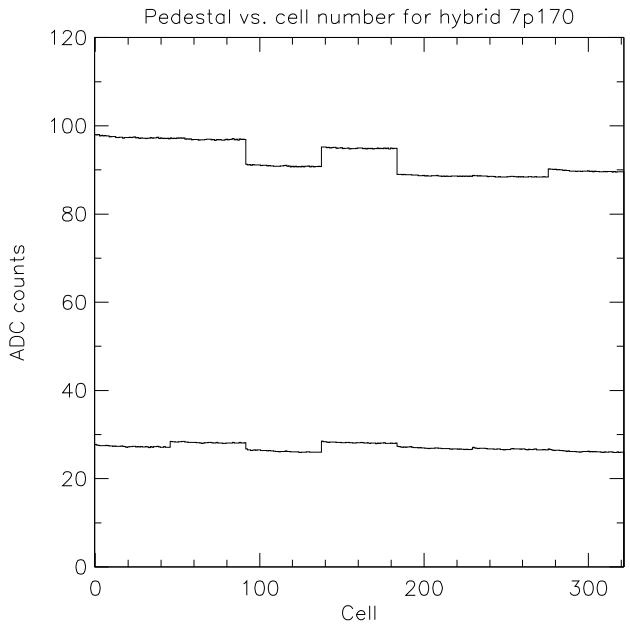
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

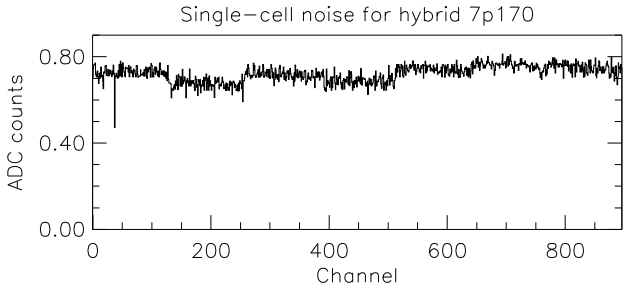
Pedestal vs. Pipeline Cell ID

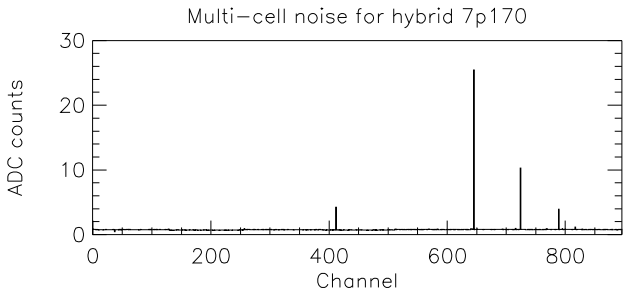


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

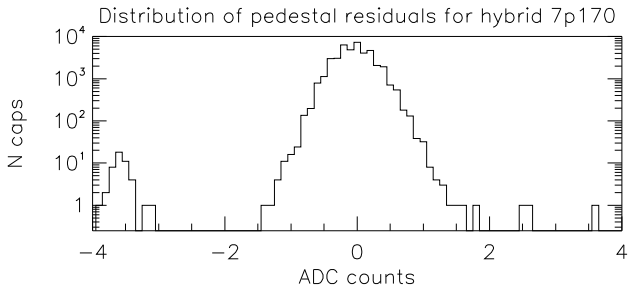
RMS Noise

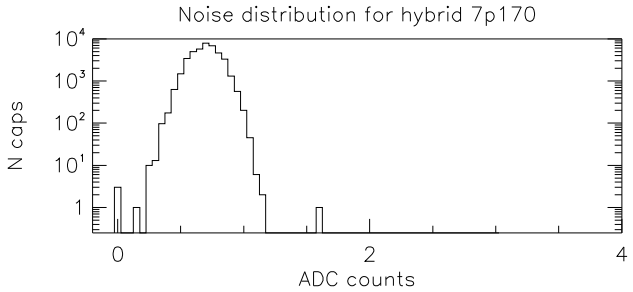




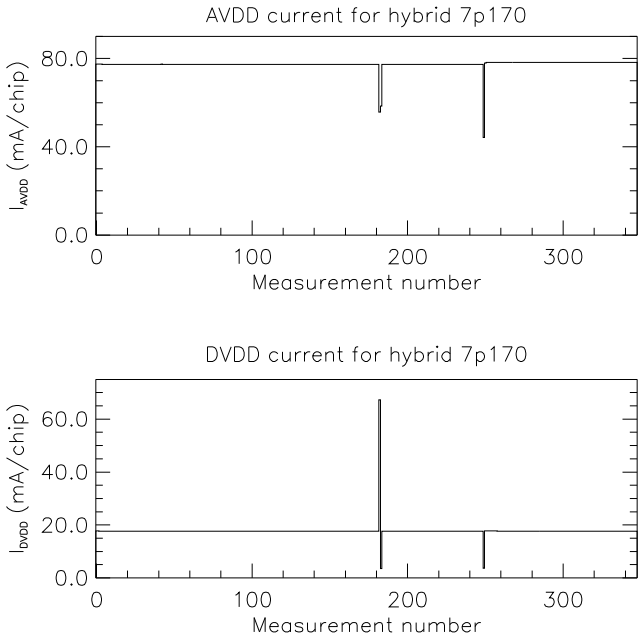
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in