Hybrid 7p45 Traveler

June 27, 2000

1 Connectivity

Repairs on shorts: PDR2 - AVDD2 :cur tracee and bypassed with soldered wire.
Fixes for opens: PRD2 and L1 with soldered wires.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P45 has die: 207-025 207-027 207-028 207-029 207-030 207-031 207-032

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p45 classification info. Created 08:52:46 06/26/00

Hybrid 7p45 quality: fair*
Chip classification: fair* good good fair fair good good
Bad channels (chip-channel): 0-2 0-3 0-84 4-2 4-19
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-11-84 0-19-84 0-20-84
   0-26-84 0-29-84 0-39-84 3-33-96 3-4-96 3-41-96
Channels at pedestal needed for DCMS: 27.7 32.7 29.7 30.3 29.6 30.7 32.5
```

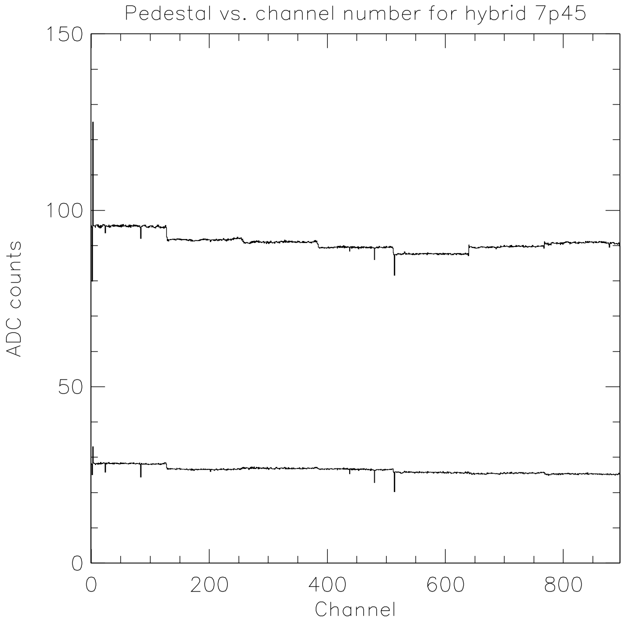
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

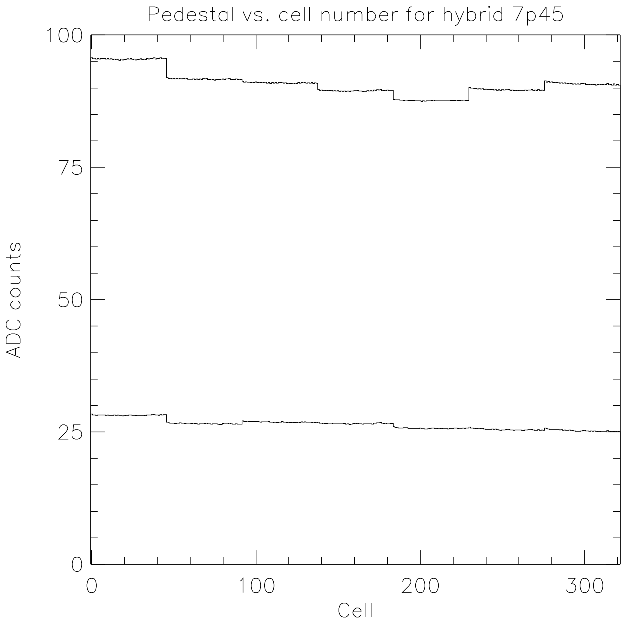
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

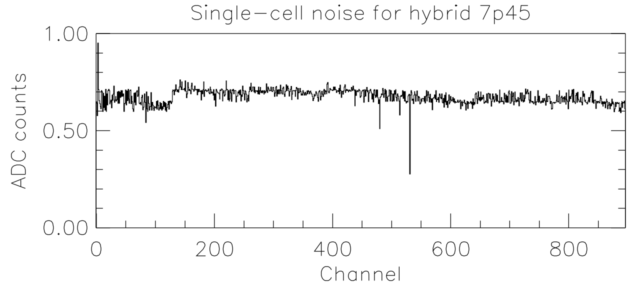
Pedestal vs. Pipeline Cell ID



6 Noise

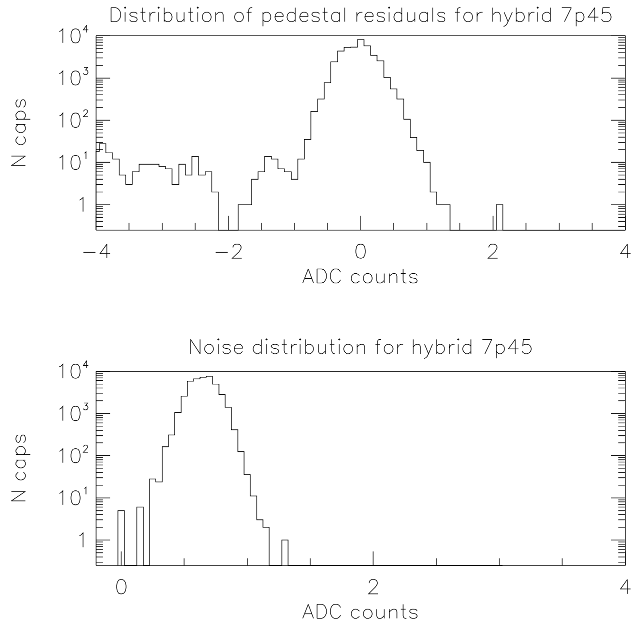
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in