# Hybrid 7p5 Traveler

May 22, 2000

## 1 Connectivity

Repairs on shorts:
Fixes for opens:

## 2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P5 has die: 076-016 076-018 076-019 076-021 076-022 076-023 076-026

## 3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p5 classification info. Created 11:51:36 05/19/00

Hybrid 7p5 quality: fair
Chip classification: good fair good fair good good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-9-52 3-1-18 3-38-127
   3-39-41 3-44-15 3-45-6 3-7-45
Channels at pedestal needed for DCMS: 29.6 32.6 30.6 30.5 31.6 30.7 30.5
```

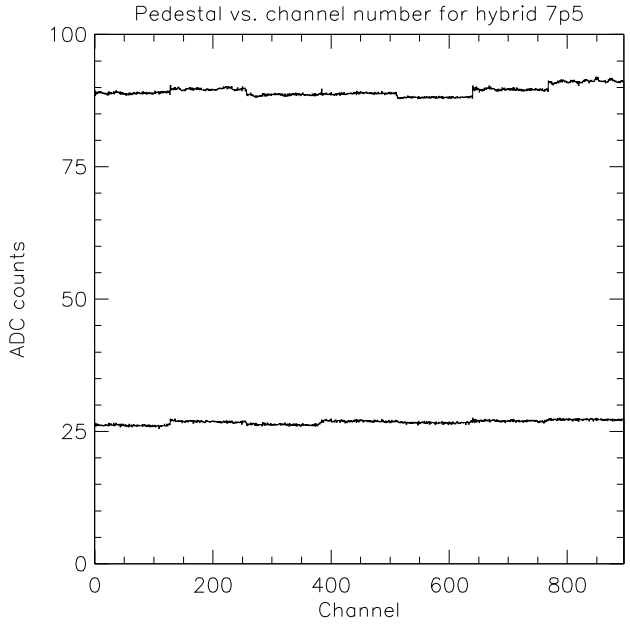
## 4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

# 5 Pedestal

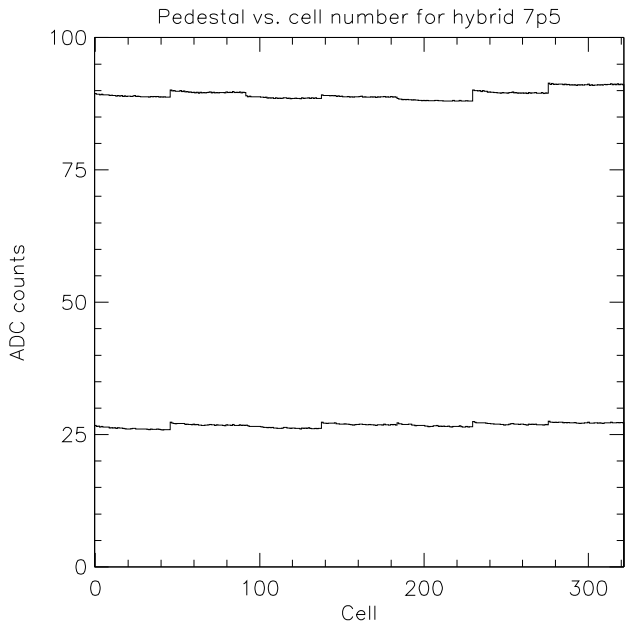
The following plot shows the pedestals vs. channel number with and without charge injection:

**Pedestal for each Channel**




The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

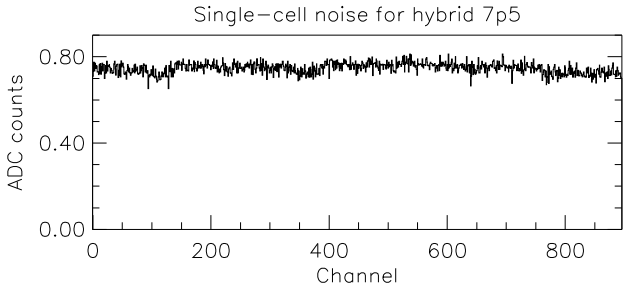
**Pedestal vs. Pipeline Cell ID**

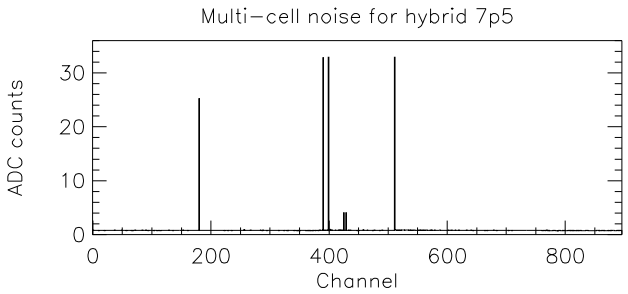


# 6 Noise

The following plots show the single-cell and multi-cell RMS noise:

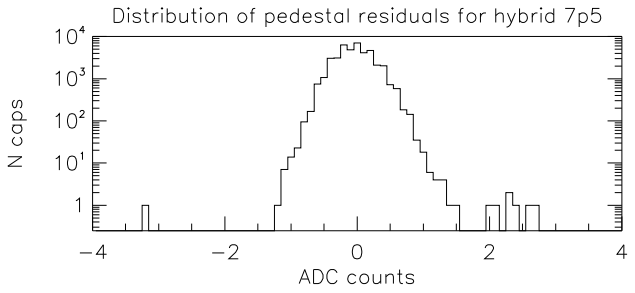
**RMS Noise**

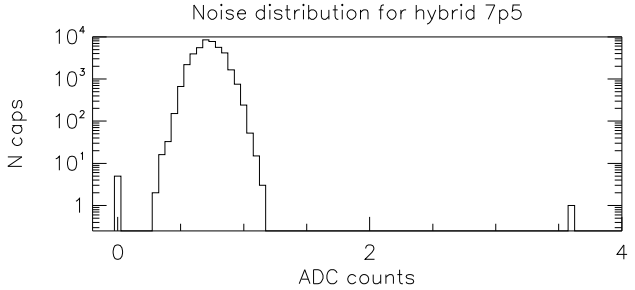


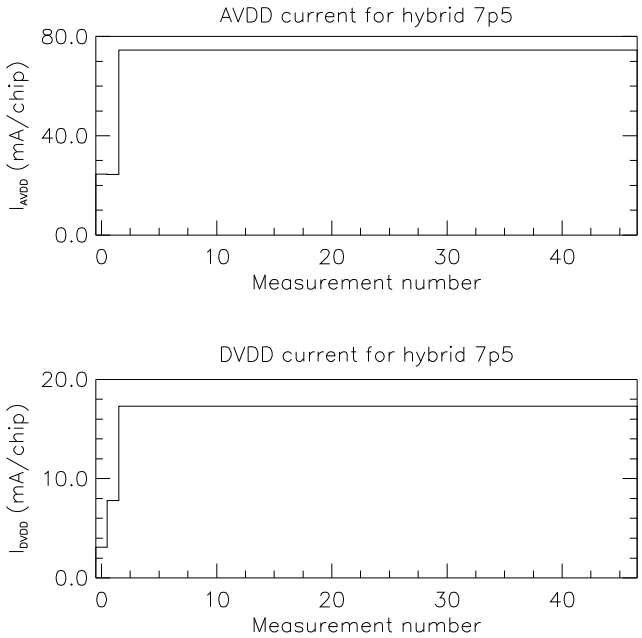

The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

**Distribution of Pedestals and Noise**



# 7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

**Supply Currents During Burn-in**