Hybrid 7p57 Traveler

June 30, 2000

1 Connectivity

Repairs on shorts: TN-BN: cut traces and bypassed with soldered wires.

Fixes for opens: TN, BN open on hybrid. Fixed

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P57 has die: 207-033 207-035 207-036 207-037 207-038 207-039 207-040

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p57 classification info. Created 11:53:16 06/30/00

Hybrid 7p57 quality: fair
Chip classification: good fair fair fair fair fair fair
Bad channels (chip-channel): 1-81 2-83 3-118 5-3 6-22 6-57
Bad cells: none
Random bad capacitors (chip-cell-channel): 4-40-103
Channels at pedestal needed for DCMS: 29.6 32.7 29.9 30.8 31.6 29.4 28.8
```

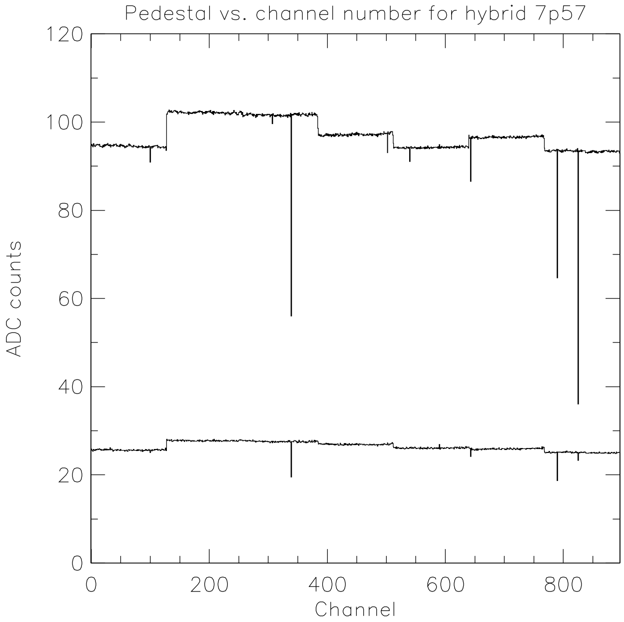
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

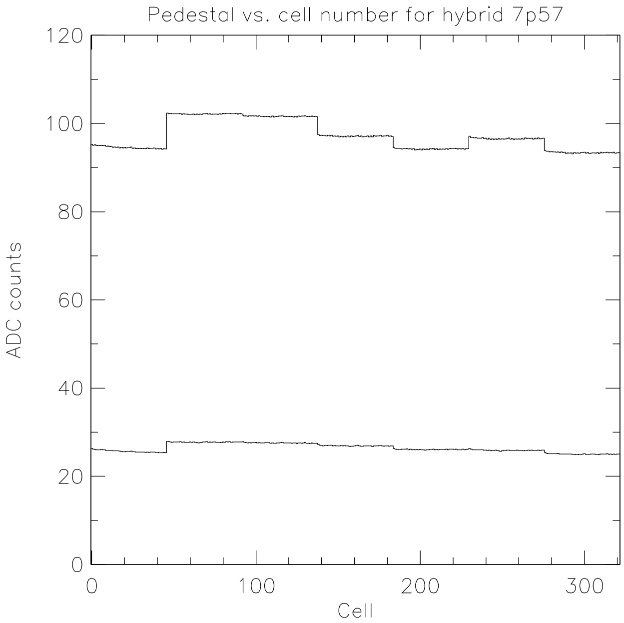
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

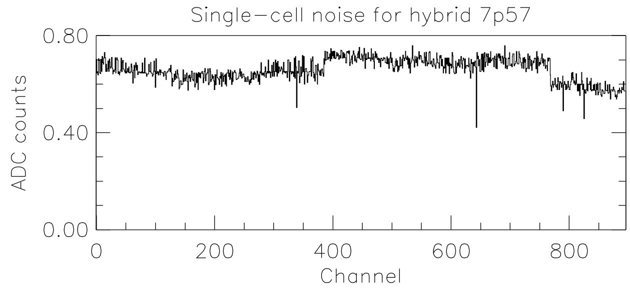
Pedestal vs. Pipeline Cell ID

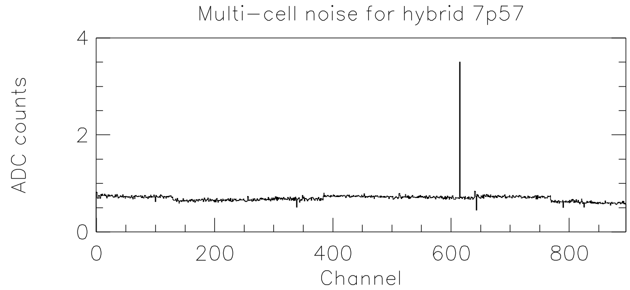


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

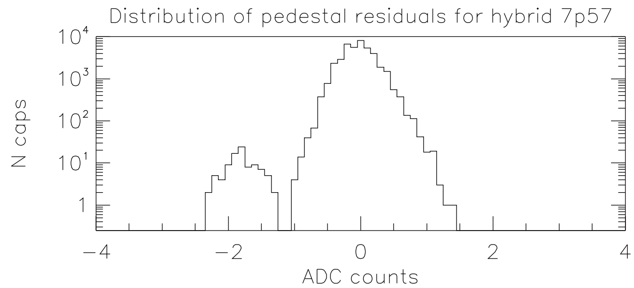
RMS Noise

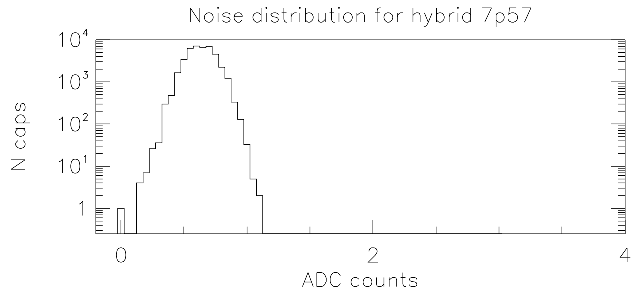




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in