Hybrid 7p62 Traveler

June 8, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens: AVDD on chip 7 w/ solder wire.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P62 has die: 243-084 243-085 243-093 243-094 243-100 243-101 243-102

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p62 classification info. Created 09:28:40 06/08/00

Hybrid 7p62 quality: fair
Chip classification: good good good good good fair good
Bad channels (chip-channel): 5-54 5-55
Bad cells: none
Random bad capacitors (chip-cell-channel): 5-16-66 5-45-13
Channels at pedestal needed for DCMS: 30.6 31.7 31.7 31.6 28.8 30.6 31.6
```

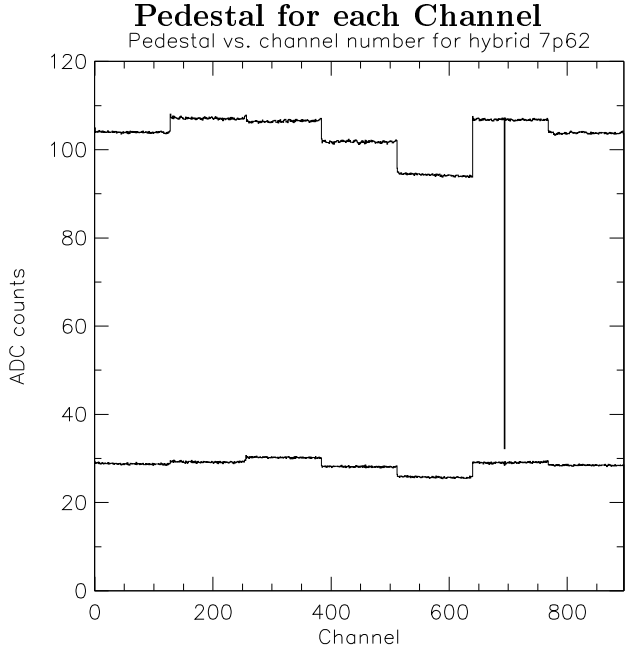
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested. Chip 5 replaced.

5 Pedestal

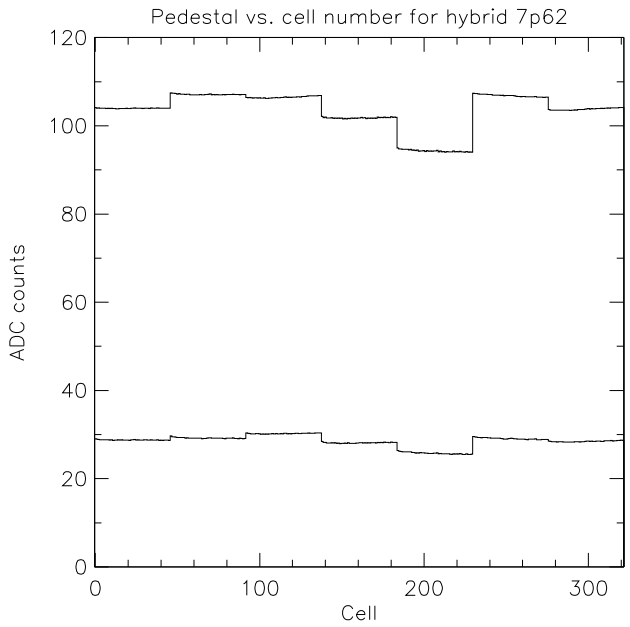
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

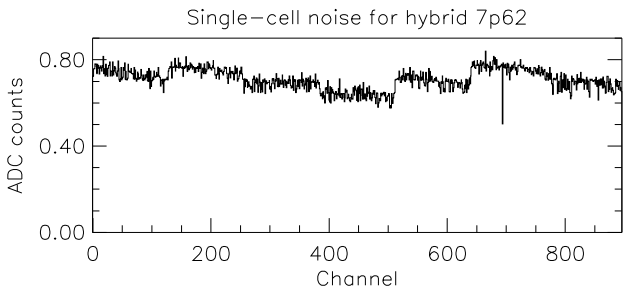
Pedestal vs. Pipeline Cell ID

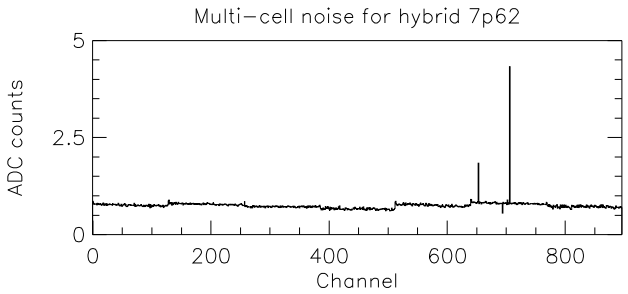


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

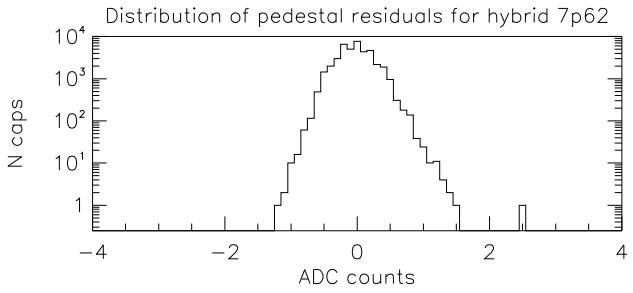
RMS Noise

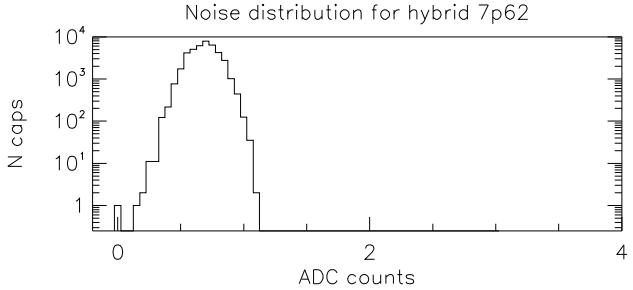




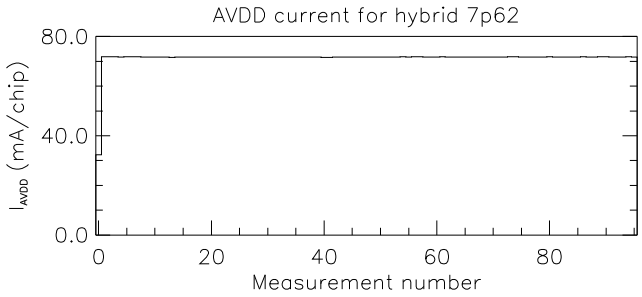
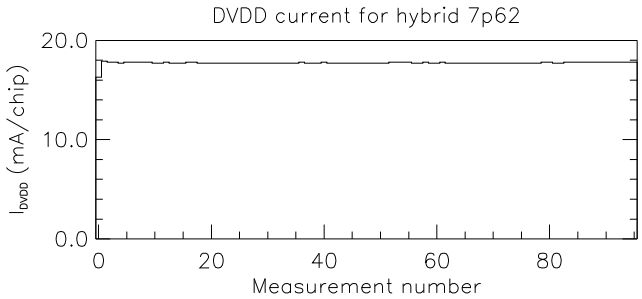
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in