Hybrid 7p74 Traveler

May 26, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens: AVDD2, Islope chip4, Islope chip5 with soldered wires.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P74 has die: 238-119 238-120 238-121 238-122 238-123 238-125 238-126

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p74 classification info. Created 09:15:19 05/26/00

Hybrid 7p74 quality: fair*
Chip classification: good good good fair fair* good fair
Bad channels (chip-channel): 3-65 3-97 4-75 4-79 4-104 4-124
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-35-64 4-37-104 4-40-104
   4-40-105 4-42-104 4-44-104 4-7-104 4-7-105 6-15-94 6-20-94 6-23-94
   6-25-94 6-27-94 6-3-94 6-36-94 6-36-95 6-37-94
Channels at pedestal needed for DCMS: 30.7 32.6 32.6 30.6 33.2 32.5 30.6
```

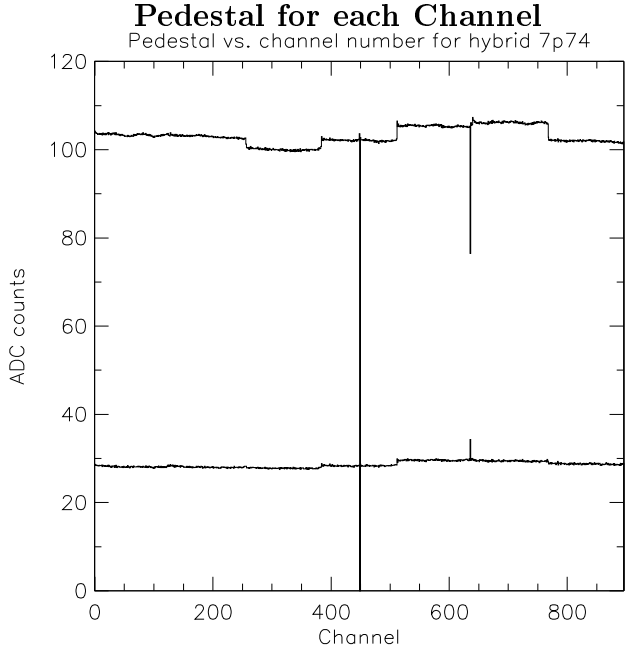
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

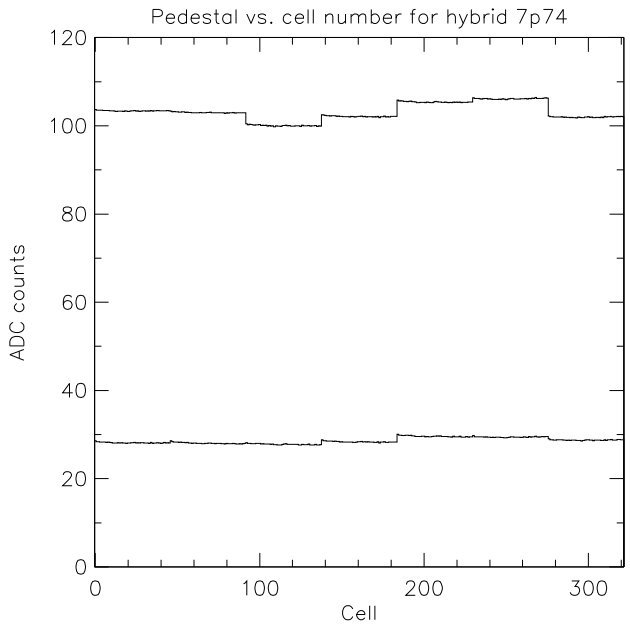
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

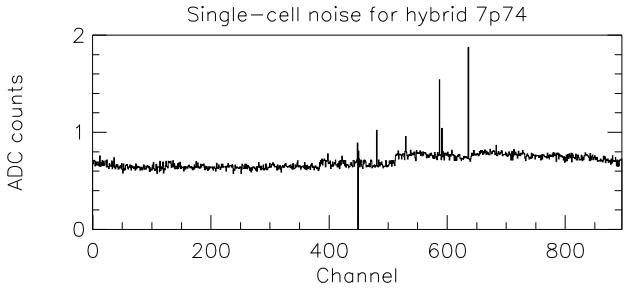
Pedestal vs. Pipeline Cell ID

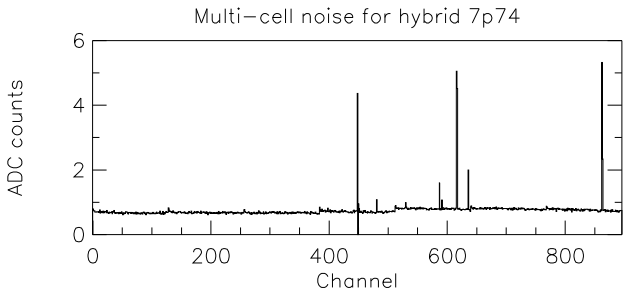


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

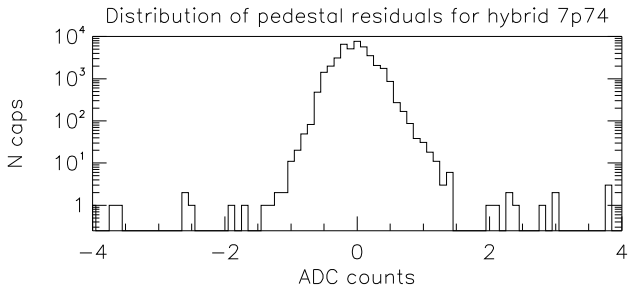
RMS Noise

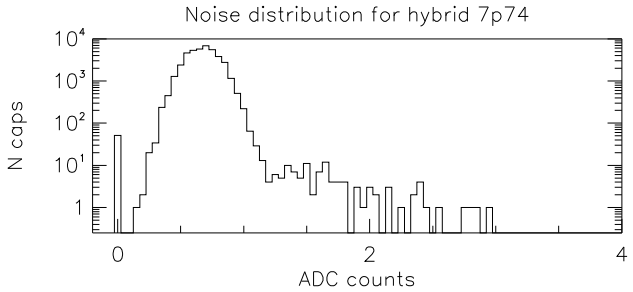




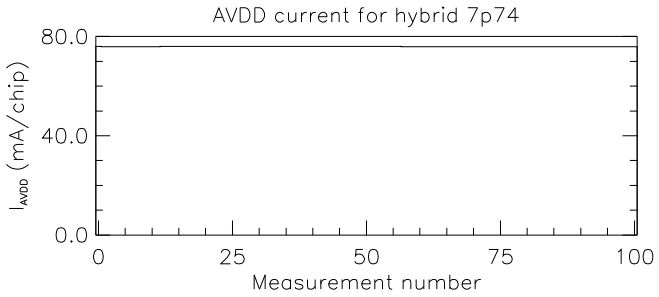
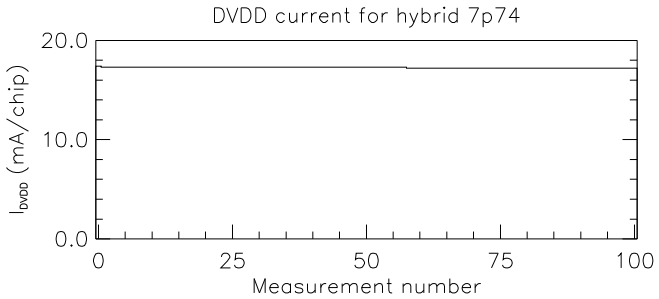
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in