Hybrid 7p84 Traveler

June 16, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens: HV+ open in hybrid.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P84 has die: 231-066 231-072 231-073 231-080 231-085 231-102 231-111

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p84 classification info. Created 09:37:44 06/08/00

Hybrid 7p84 quality: fair
Chip classification: fair fair good fair fair fair fair
Bad channels (chip-channel): 0-42 1-79 3-38 3-75 4-72 5-113 6-41
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-21-62 1-29-62 1-4-62
Channels at pedestal needed for DCMS: 30.7 29.8 32.6 30.7 31.6 29.7 31.7
```

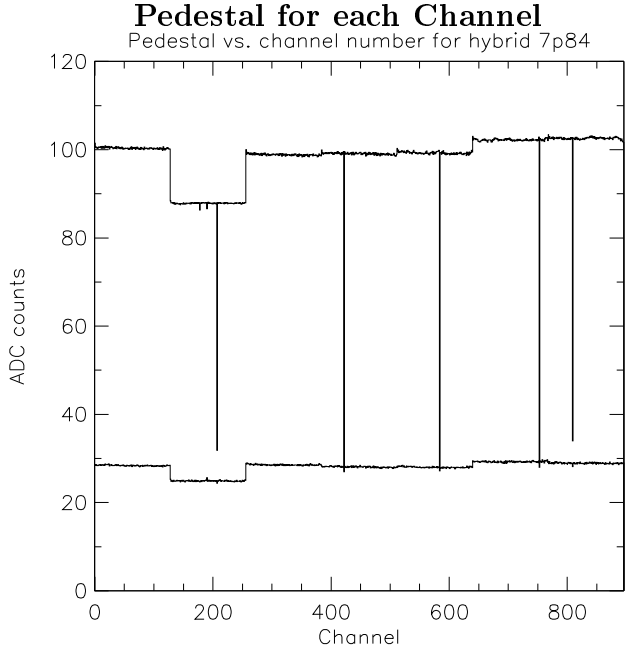
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

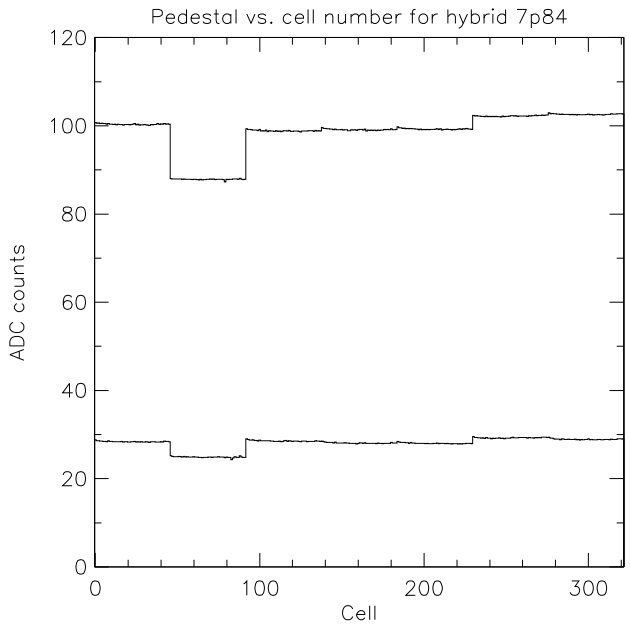
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

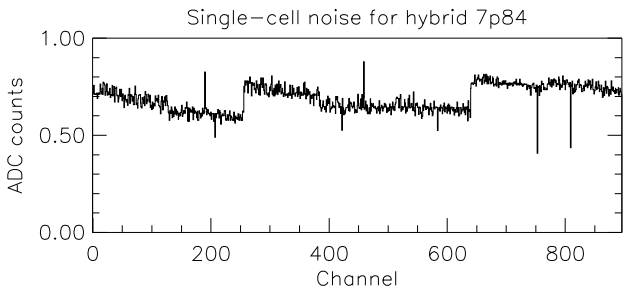
Pedestal vs. Pipeline Cell ID

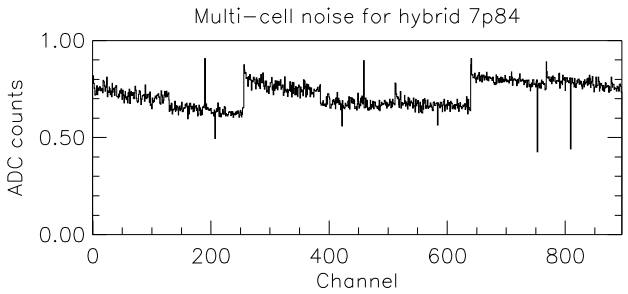


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

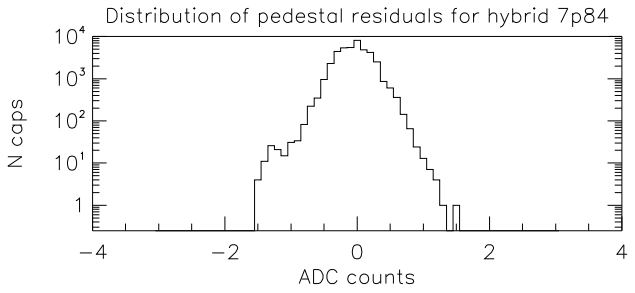
RMS Noise

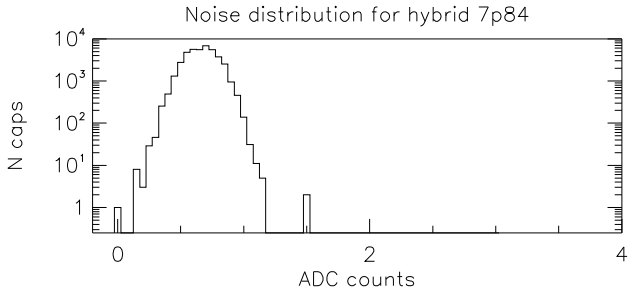




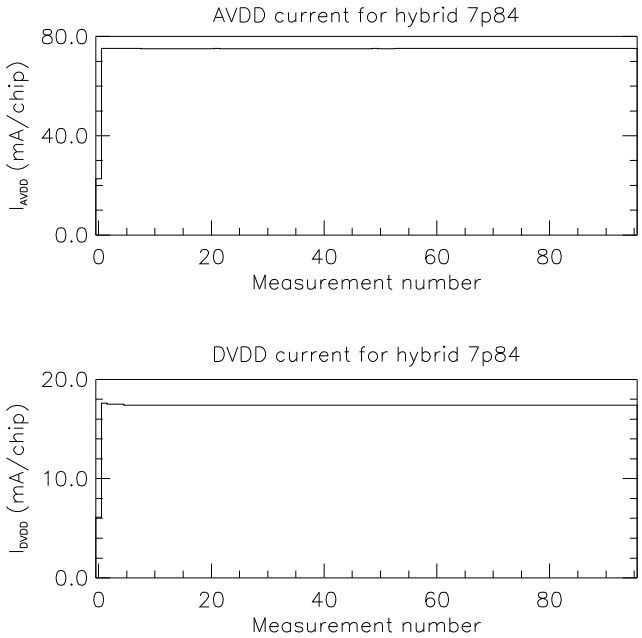
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in