Hybrid 7p9 Traveler

October 20, 1999

1 Connectivity

Repairs on shorts: Extra wire bond between DGND and DVDD removed

Fixes for opens: Bus 4B open to chip 4; fixed with wirebond

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7P9 has die: 120-037 120-040 011-020 119-005 119-006 119-013 119-020

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7p9 classification info. Created 10:50:08 10/20/99
% Revised 11:09 10/20/99 after inspection of data to verify
% that only 1 channel (not 3) were bad on last chip   AFS/IGV
%
% Classified as "data source" due to slightly too many bad chs.
% but otherwise OK... could be used in a pinch if needed.
%

Hybrid 7p9 quality: data-source (8 bad channels in 7 chips)
Chip classification: fair fair good fair fair fair fair
Bad channels (chip-channel): 0-30 1-33 3-80 3-81 4-47 5-0 5-1 6-64
Bad cells: none
Random bad capacitors (chip-cell-channel): 4-13-47 5-34-0 5-34-93 5-42-0 6-2-118
```

```
Channels at pedestal needed for DCMS: 35.0 40.6 36.6 36.6 35.5 34.6 39.0
```

4 Comments

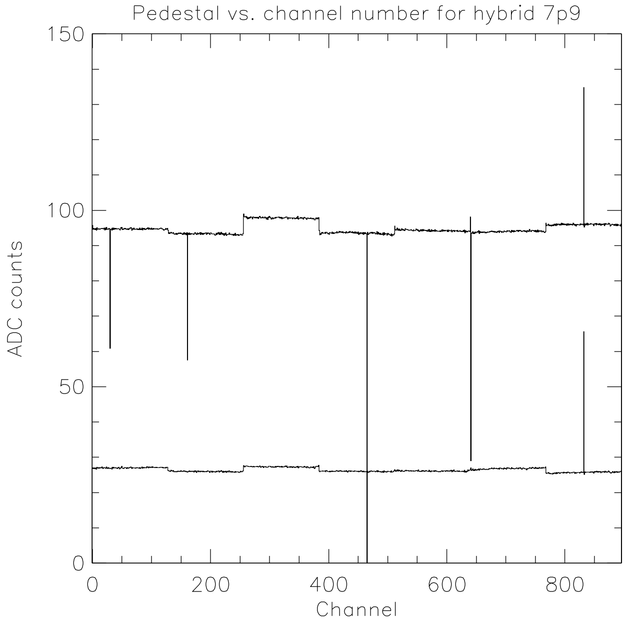
Chip 3 replaced with 11-20

Nearest-neighbor sparsification flagged 6-63, 6-64, and 6-65 as bad but this appears to be a bug – only 6-64 is actually bad, so should pass this test.

5 Pedestal

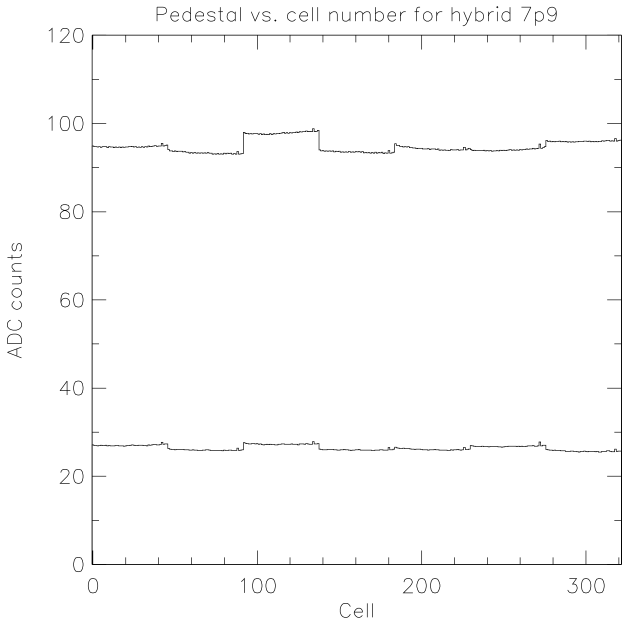
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

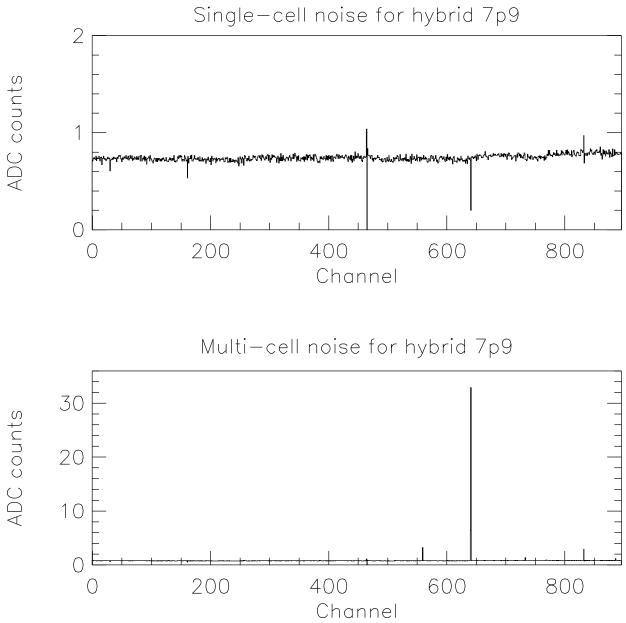
Pedestal vs. Pipeline Cell ID



6 Noise

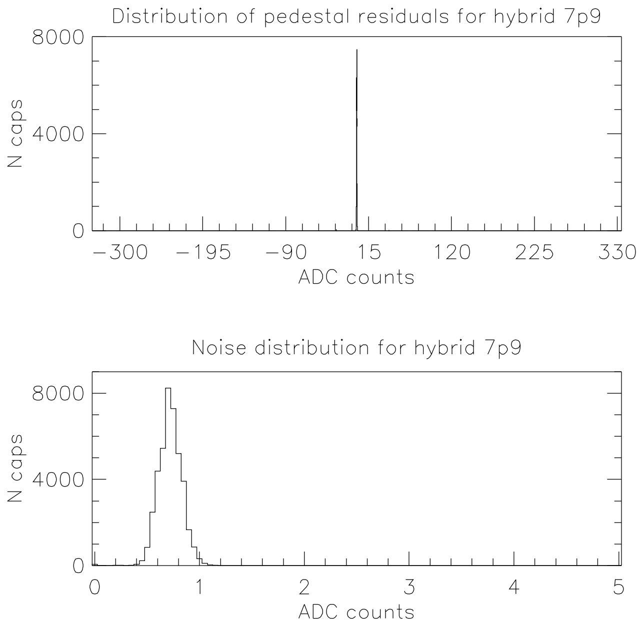
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in