Hybrid 7z103 Traveler

February 3, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7Z103 has die: 226-079 226-080 226-081 226-083 226-085 226-086 226-087

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7z103 classification info. Created 10:42:37 02/02/00

Hybrid 7z103 quality: fair
Chip classification: good fair good fair good good good
Bad channels (chip-channel): 1-19
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-14-18 1-18-18 1-21-18
   1-23-18 1-25-12 1-35-18 3-16-104 3-16-105 3-17-105 3-20-104 3-20-105
   3-21-105 3-23-104 3-23-105 3-25-104 3-25-105 3-27-104 3-27-105 3-3-105
   3-36-104 3-36-105 3-37-105
Channels at pedestal needed for DCMS: 34.7 32.7 36.7 31.6 32.7 34.7 35.7
```

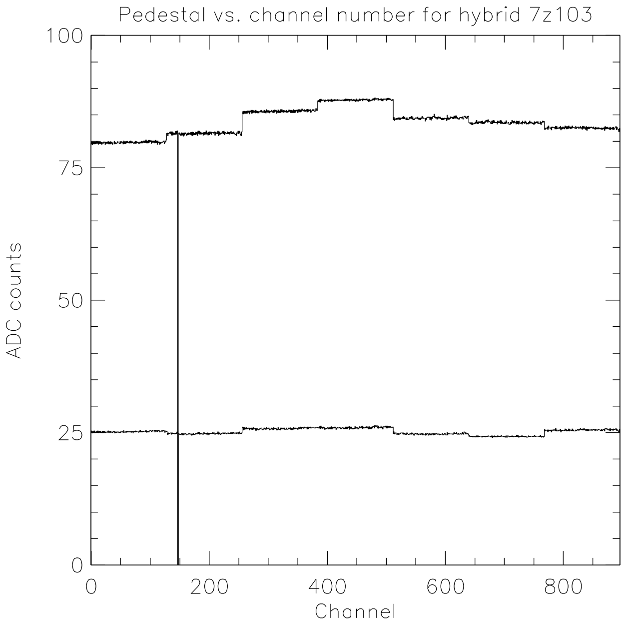
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

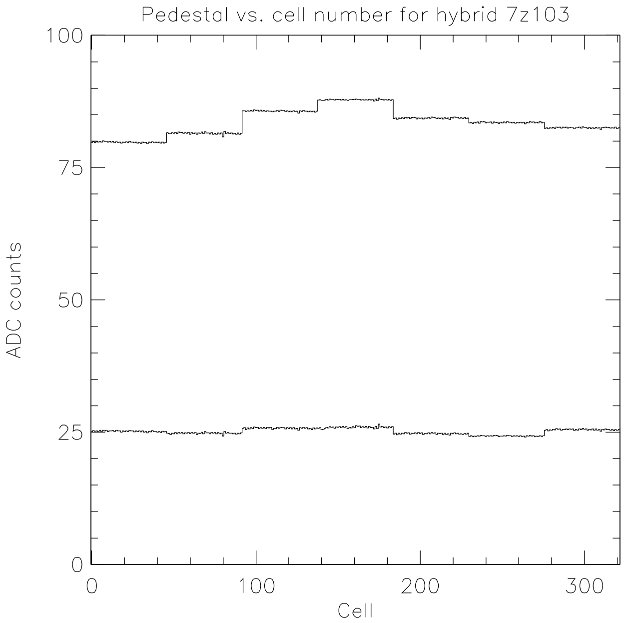
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

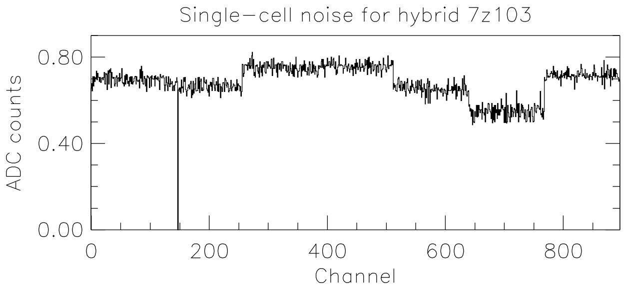
Pedestal vs. Pipeline Cell ID

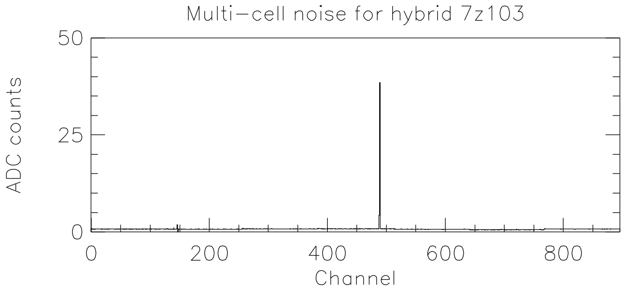


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

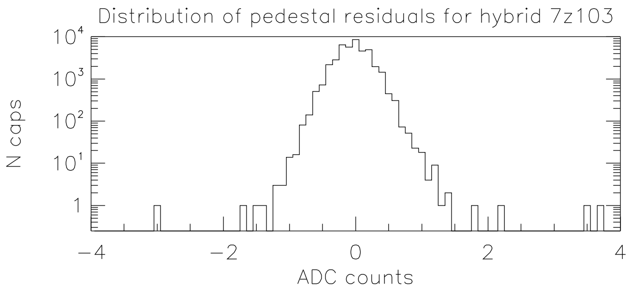
RMS Noise

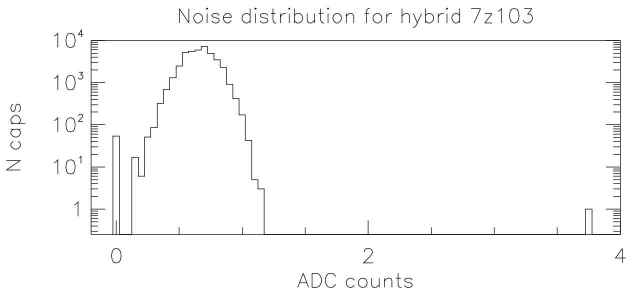




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in