Hybrid 7z182 Traveler

February 3, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7Z182 has die: 226-026 226-027 226-030 226-031 226-032 210-085 210-096

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7z182 classification info. Created 09:38:40 01/31/00

Hybrid 7z182 quality: fair
Chip classification: good good good fair fair good fair
Bad channels (chip-channel): 3-7 6-20 6-100
Bad cells: none
Random bad capacitors (chip-cell-channel): 4-29-17 6-0-21 6-17-83
   6-9-19
Channels at pedestal needed for DCMS: 33.7 32.6 35.7 30.7 31.7 33.7 32.7
```

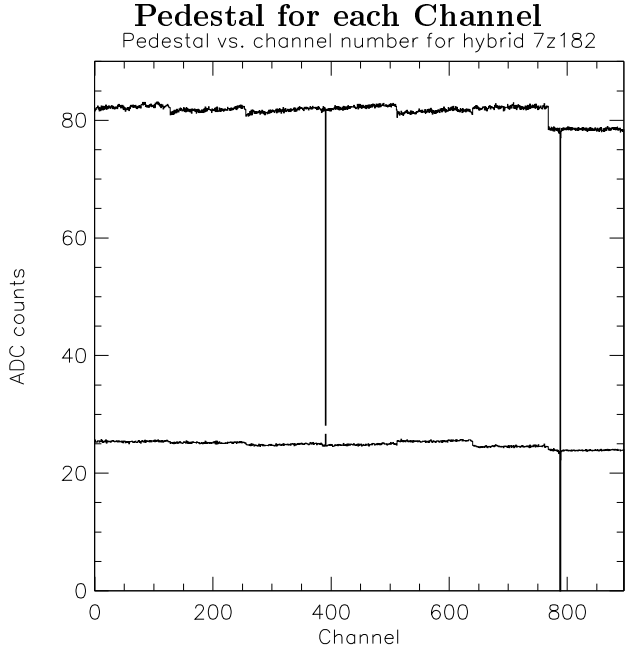
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

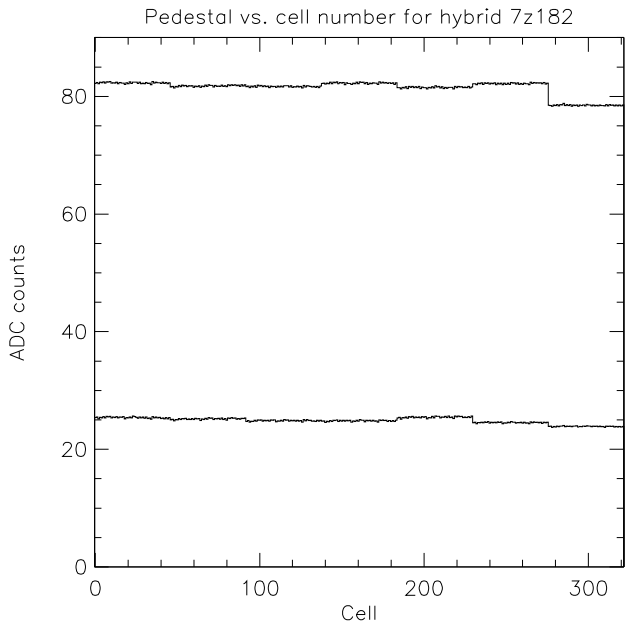
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

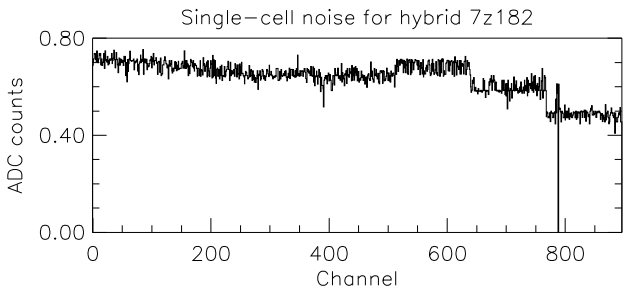
Pedestal vs. Pipeline Cell ID

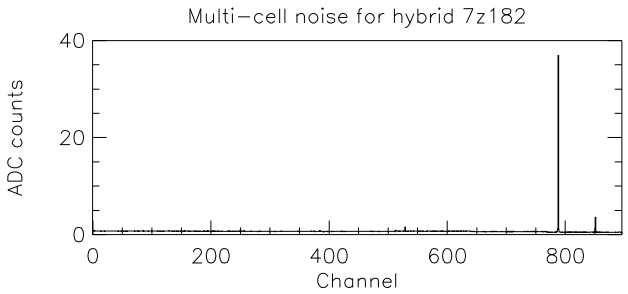


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

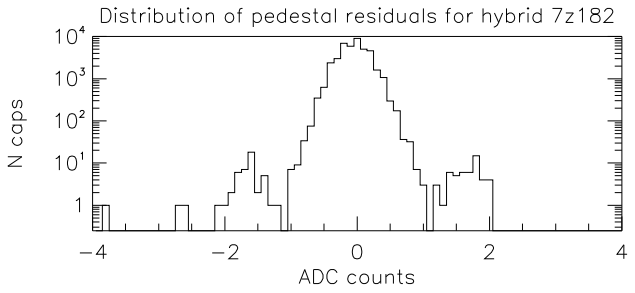
RMS Noise

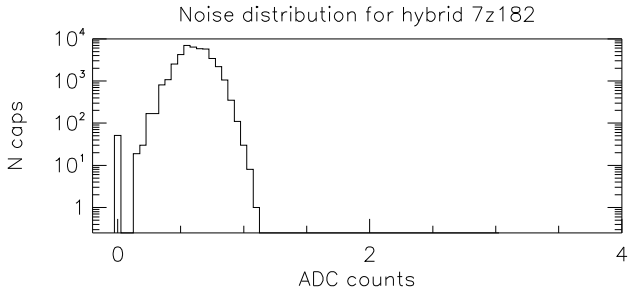




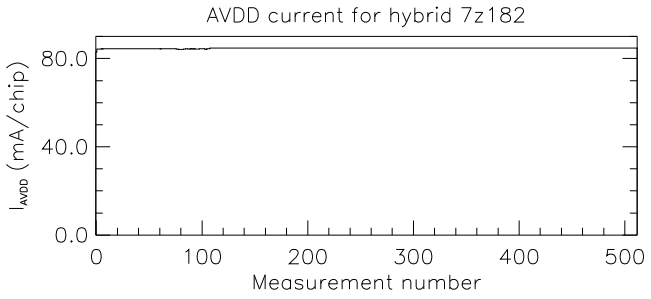
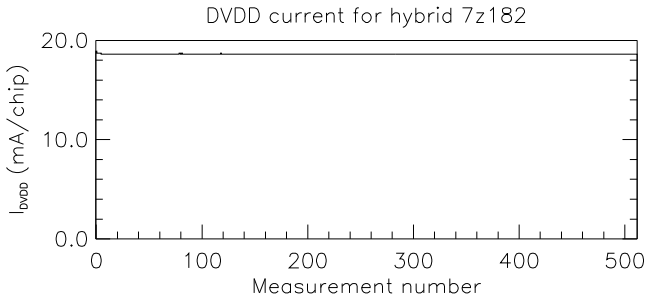
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in